

Silicon Divisions within CEA-Leti

CEA is a French government-funded technological research organisation. Drawing on its excellence in fundamental research, its activities cover three main areas: Energy, Information and Health Technologies, and Defence and Security. As a prominent player in the European Research Area, with an internationally acknowledged level of expertise in its core competencies, CEA is involved in setting up collaborative projects with many partners around the world.

Three institutes within CEA's Technological Research Division are focused on increasing industrial competitiveness through technological innovation and technology transfers: **CEA-Leti**, focused on microelectronics, information and healthcare technologies, **CEA-List**, dedicated to technologies for digital systems, and **CEA-Liten**, devoted to new energy technologies.

CEA-Leti is focused on creating value and innovation through technology transfer to its industrial partners. It specializes in nanotechnologies and their applications, from wireless devices and systems, to biology, healthcare and photonics. NEMS and MEMS are at the core of its activities. An anchor of the MINATEC campus, CEA-Leti operates 8,000-m² of state-of-the-art clean room space on 200mm and 300mm wafer platforms. It employs 1,400 scientists and engineers and hosts more than 190 Ph.D. students and 200 assignees from partner companies. CEA-Leti owns more than 1,700 patent families. For more information, visit http://www.leti.fr.

Within CEA-Leti, Silicon Technologies and Components research activities are shared between two divisions gathering together around 550 researchers. **The Silicon Technologies Division** operates three different technological platforms: the MOS200 platform providing 200mm MOS wafer processing, which can be applied to both semiconductor and microsystems devices; the MEMS200 platform producing non-CMOS micro-electromechanical systems (MEMS); and the 300mm nanotechnology and 3D integration platform allowing complete 3D-integration demos using TSV middle and last processes. **The Silicon Components Division** carries out research on nanoelectronics and heterogeneous integration on silicon and is focusing on two mains areas: on-going shrinking of CMOS devices to extend "Moore's Law" for faster, less-expensive computing power, and the integration of new capabilities into CMOS, such as sensors, imaging technology, and new types of memory, to enable new applications.



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2011 Facts & Figures



553 Permanent Researchers114 Industrial Residents97 PhD Students12 Post-Docs



200 & 300mm Platforms for CMOS and MEMS

7,500 m² Clean Rooms 500 Process Tools Continuous Operation



107 Patents Filed in 2011431 Scientific Papers Published in 2011



12 Common Laboratories2 Startup CompaniesCreated in 2011

Credits CEA-Leti G.Cottet & Ipdia



Annual Research Report 2011 Silicon Technologies & Components



2011 Year of Maturity

Jean-René Lèquepeys

Interview

Head of Silicon Components Division

One year ago, at the start of 2011, we created the Silicon Components Division to improve our offer to our industrial partners. The mission of this new division is to provide industry-relevant solutions in extended domains like CMOS. memories, energy, MEMS&NEMS or 3D integration. The main driver of our research remains to help and support our customers to build valuable and differentiated products though innovation.

The Silicon Components Division is organized to cater to smart-systems integration requirements by linking the technological bottom-up approach to a top-down applications-driven approach. Our three departments are:

■ MOS Department: its mission is to simulate, model, develop, demonstrate and test new generations of components for sub-20nm CMOS, memory, power and photovoltaic devices.

■ MEMS Department: its mission is to design and develop innovative microsystem components (sensors, actuators and RF components).

3D Integration Department: its mission is to develop all technology modules for both 3D high density and high flexibility integration.

The Silicon Components Division has strong connections with the other Leti divisions. We interact daily with the Silicon Technologies Division which operates the clean rooms, and we exchange closely with Systems and Design divisions to exploit leverage between our expertise domains to further innovation.

In 2011, the launch of the new organization has been followed up by real results. We reached a new record of scientific papers published in the top ranking conferences and journals, we submitted 72 patents and, above all, we now collaborate with new customers.

In particular, in 2011, we extended our partnerships to all microelectronics production sites located in France and we became the core of a national program aiming to support innovation in advanced manufacturing through applied research programs for promising applications.

Among our key milestones reached in 2011 I'd like to point out the most significant for me: the selection by ST-Ericsson of the planar fully depleted silicon on insulator (FD-SOI) technology for use in future mobile platforms. With our partners, Soitec, STMicroelectronics and IBM, we have invested over several years in the development of FD-SOI technology, and we have recently demonstrated the strong differentiation of this technology versus conventional bulk CMOS for high-performance and lowpower on several IPs at 28nm and below. This success underscores the capability of Leti to nurture innovative technologies and to transfer them to industry.

Likewise, significant achievements to address the energy challenge have been demonstrated in 2011, as we continue to invest in manpower and tools for PV and 200mm GaN on silicon for power devices.

This annual report highlights our key achievements of 2011, in the various domains that we operate. If you require any further information, please feel free to contact us.

We couldn't have accomplished what we have without the expertise, the passion and the commitment of the Silicon Components division teams. I would like to take this opportunity to thank all of them.

In conclusion, I am confident in our ability to provide our partners with valuable solutions and expertise and I invite you to join us.





Fabrice Geiger

Head of Silicon Technology Division

Since March 2011 reorganization our division maintains its efforts to improve cycle-time and quality-of-service. Results are here and our 200mm and 300mm lines can compare to industrial standards. Our strong investment policy has continued to improve the reactivity and effectiveness of Leti's different technological platforms.

The role of two first technological platforms is to bridge the gap between upstream research and development of nanotechnology new micro and applications. The MOS200 platform provides 200mm CMOS wafer processing, both which can be applied to semiconductor and microsystem devices. The MEMS200 platform produces non-CMOS Micro-ElectroMechanical Systems (MEMS). Both platforms are focused on the More than Moore initiative to develop semiconductor capabilities. new An innovative cleanroom shuttle system now links the two platforms to add process flexibility and faster processing.

The third platform is dedicated to 300mm nanotechnology and 3D integration. 3D innovative approach integrates various micro- electronics objects together in order to juxtapose complementary functions (such as sensing, storing, processing, actuation, communication and energy scavenging) advanced providing system hence solutions in 3 dimensions. Inaugurated in January 2011, this line is now fully operational and is now open to our customers for prototyping through the Open3D service.

Together, the three platforms have 7,500m2 of cleanroom space, 500 process tools and a combined staff of more than 450; they run industry-like operations, 24 hours a day, 7 days a week, all year round.

All research carried out in our cleanrooms benefits from the Nano-Characterization Platform, which is located on the MINATEC campus. This platform, unique in Europe, covers a large domain of competencies, including electron microscopy, X-ray diffraction, surface analysis and sample preparation.

Our Silicon Technologies division is organized according six departments.

■ Three Process Departments: their missions are to realize generic process steps for all projects and to develop innovative processes to provide state-ofthe-art solutions to internal and external customers. departments Those are focused on patterning, deposition, and surface treatments. Their research activities in collaboration with key universities allow LETI's advanced position in the future.

■ A Characterization Department: this department realizes all measurements and observations to characterize process steps, materials or components. This department also has a research activity to maintain its level of excellence.

Two Support Departments: one is in charge of the planning, the interface with internal divisions or external customers as well as methods, training and clean-concepts. The other is responsible for facilities operations and engineering.





Simon Deleonibus

Chief Scientist, CEA Research Director

We have completed the 2011 Annual Silicon Components and Technologies Scientific Report which is the second of the regular yearly edition. This booklet contains 69 short research summaries of 1 page in the different working themes Silicon Components of the and Technologies Divisions (Silicon Divisions) activities. Our researchers highlight their results, obtained in 2011, and point out the main publications referred to. Their efforts illustrate the strong collaborative work of the Components and Silicon Technologies Divisions (Silicon Divisions) with the various Research Institutes, Universities and Companies of the MINATEC Campus, at the local, national and international levels.

The researchers of the Silicon Divisions are at the very heart of the innovation that drives LETI's activities. They have directly and actively contributed to write the 2011 Scientific Report without neglecting the contribution of partner institutions. The Report is arranged following a thematic rather than the functional organization of the Silicon Divisions. The document is divided in 8 main chapters: Core & Beyond CMOS, Memories, Patterning, Power Electronics Passive and 8, Photovoltaic, RF Components, MEMS Actuators & Sensors & their Reliability, 3D Integration & Packaging, and Physical & Chemical Characterization.

In 2011, the Silicon Divisions produced 431 publications among which more than 119 in peer reviewed journals, reaching impact factors as high as > 33 and 270 grade A oral communications at international conferences. We are particularly proud to highlight the recognition of the excellence of our latest research results. Our peers' interest to the excellence of our results has brought us a total of forty-one added Awards.

In 2011, 7 awards have been delivered to our assignees and their coworkers mostly in the frame of collaborative work. After the 2009 IEEE Roger Haken Award, the Silicon Divisions obtained another prestigious recognition that I wish to particularly point out: the Best Student Paper Award of the 2010 VLSI Technology Symposium was given at the 2011 edition to Laurent Brunet et al. for the paper entitled "New Insight on VT Stability of HK/MG Stacks with Scaling in 30nm FDSOI Technology". Four other Best Paper Awards were obtained as well international conferences: 2011 at International Workshop on Microscopy of Semiconducting Materials (Thibault Denneulin et al.), 2011 Sematech PCC Workshop (Thy Ti Thuy Nguyen et al.), 2011 International Workshop on Variability (Jerôme Mazurier et al.), Intermag 2011 (Michel Quinsat et al.).

We were, as well, honored by two Technical Awards from public institutions and private companies:

1) the French-German Chamber of Commerce and Industry for the French-German Prize for Economy to the LETI/FhG/SOITEC consortium on Concentration PV leading the Solarbond Project (the Award is sponsored by French and German major companies),

2) the ST Microelectronics Silver Award for successful transfer of FDSOI.



These recognitions have been awarded to our scientists which underlines the trust of our peers in our strong involvement into the future. Their achievements have been obtained thanks to a strong collaborative teamwork and involvement.

Our research vocation is also to promote new spin off company creation. Two companies were spun out from CEA-LETI in 2011:

1) **Apix**, building Multi-Gas Detection based on NEMS technology and micro gas concentration integration,

2) **Wavelens**, integrating compact active lenses for autofocus and phone cameras applications.

Finally, it is our pleasure to underline these events.



Indicators of Scientific Activity & Performance

Publications

431 publications in 2011 Ratio "A grade publication/ Researcher" > 1

Prize and Awards

7 awards in 2011

- Best Student Paper Award of the 2010 VLSI Technology Symposium was given at the 2011 edition to Laurent Brunet *et al.* for the paper titled "New Insight on VT Stability of HK/MG Stacks with Scaling in 30nm FDSOI Technology",

- 2011 International Workshop on Microscopy of Semiconducting Materials (Thibault Denneulin *et al.*),

- 2011 Sematech PCC Workshop (Thy Ti Thuy Nguyen et al.),

- 2011 International Workshop on Variability (Jerôme Mazurier et al.),

- 2011 Intermag (Michel Quinsat et al.),

- 2011 French-German Prize for Economy to the LETI/FhG/SOITEC consortium on concentration PV leading the Solarbond Project,

- 2011 ST Microelectronics Silver Award for successful transfer of FDSOI.

41 added Awards among which 2005 Grand Prix Académie des Technologies, 2008 IEEE Cledo Brunetti Award, 2011 French-German Prize for Economy, 2011 Silver Medal ST Microelectronics, 29 Best Papers Awards

1 ERC Grant

Experts

71 CEA experts: 1 Research Director, 5 International Experts

18 Researchers with Habilitation qualification (to independently supervise doctoral candidates)

1 IEEE Fellow and 3 IEEE Seniors Members

Scientific Committees

2 Journal Editors: TED and Europhysics Journal Applied Physics,

7 researchers involved in ITRS (The International Technology Roadmap for Semiconductors),

38 members of Technical Programs and Steering Committees in major conferences: IEDM, VLSI Technology Symposium, IRPS, ESSDERC, SSDM, ECTC...

Awards committees: IEEE Paul Rappaport Award, SEE & IEEE Brillouin-Glavieux Award, IEEE Cledo Brunetti Award, European Research Council Panel, Nanosciences Foundation Board, IEEE ED Society Administration Committee

International Collaborations

Collaborations with more than 50 universities and institutes worldwide

CALTECH, University of Stanford, University of Berkeley, Tokyo Institute of Technology, University of Tokyo, ...





PhD Degrees Awarded in 2011

Mathieu LIONS

University Pierre et Marie Curie - Paris VI

Synthesis and Characterization of Ultra-Thin Poly-Crystalline Diamond Films for Silicon-On-Diamond Applications

Diamond film integration in novel microelectronics architectures (Silicon-On-Diamond) to replace SOI substrate insulated buried layer, is a way to increase heat management. To synthesize ultrathin polycrystalline diamond (<150 nm), with maintained electrical properties, is challenging. To obtain such homogeneous films on 2" substrate with a reproducible procedure, a MPCVD reactor was modified and the synthesis protocol optimized. To synthesize fully covering films, the growth first steps were modeled. Moreover, it has been shown that the stabilisation stage strongly influence the initial nanocristals density. This stage was optimized to get initial nanocristals density over 1011 cm2. The first thermal conductivity measurements on these films were about 5 W/m.K. Indeed, the influence of the grain boundaries on the thermal conductivity dropping was bringing to light by a nanostructure modeling. The nanostructure modification allows getting thermal conductivity above 20 W/m.K. On the contrary, the electrical resistivity is related to the film chemical quality. An improved synthesis leads to electrical resistivities above 1015 Ohm.cm. Finally, different large area growth reactors were studied. Films produced with these reactors were evaluated and characterized.

Paul-Henri MOREL

University of Grenoble

Study of the Grown Silicon Nanowire 3D Integration and Physical Properties –

Fabrication of High Density Capacitors

The main focus of microelectronic industry has been to increase the number of integrated transistors in each circuit thanks to the device miniaturization. However, due to the increasing manufacturing and development costs combined with the increase of parasitic phenomena in transistors when the dimensions decrease, the microelectronic industry is now focusing on the three dimensional integration in which strategy, the circuits are stacked. The next step of this tendency will be able to consist in a component stacking inside the same three-dimensional circuit. In this context, the catalyzed CVD grown silicon nanowires are a very promising material since they can be grown with a crystalline structure without any epitaxial relationship. They can also have nanoscale dimensions without any aggressive photolithography step. We report in this thesis, the nanowire integration in high density MOS and MIM capacitors using the high developed surface of a nanowire assembly. This way, we have obtained capacitance densities of 22µF/cm² and of 9µF/cm² for MOS and MIM capacitors respectively. In this work, we present how the devices have been designed, fabricated and characterized from the nanowire growth to the complete devices. We have also studied the main steps of the nanowire integration MOS transistors for interconnects. A guided nanowire growth process has been developed and the interface quality of a low temperature deposited gate stack has been investigated. This study is based on a comparison of MOS capacitor electrical performances between catalyzed and unanalyzed silicon nanowires obtained by selective epitaxial growth. The catalyzed nanowires show a very good interface quality with a gate stack composed of alumina and titanium nitride. The technologies developed in this thesis open new opportunities for the 3D integration of devices on the same chip.

Giovanni BETTI BENEVENTI

University of Grenoble and University of Modena e Reggio Emilia

Characterization and Modeling of Phase-Change Memories

Floating-gate-based NVMs, usually named Flash memories, represent the today mainstream in the NVM market, and are expected to be the reference technology also in the near future. Nevertheless, Flash paradigm presents intrinsic physical constraints that hamper their further scaling. Among new options, one of the more interesting is the Phase-Change Memory (PCM). This Ph.D. thesis, entirely devoted to PCM, fits in this framework. One of the main goal of this research work has been the investigation of three of the key aspects of advanced solid-state memory technology development: (a) investigation of new materials, (b) advanced electrical characterization techniques and (c) modeling for comprehension of physical phenomena. A characterization study on a novel phase-change material (i.e. carbon doped GeTe) is presented for the first time. Carbon-doped GeTe promises to alleviate both of the main PCM issues, namely programming current reduction and data retention amelioration. Finally, the current-voltage behavior of crystalline PCM cells is investigated. Modeling of physics of PCM can indeed enable cell and material design, multilevel capabilities, as well as system design strategies (e.g. developing of read-window-of-budget tools) and scaling predictions.





Kiichi TACHI Grenoble University and Tokyo Institute of Technology

Physical and Technological Study of Nanowire MOS Transistors Architectures

Vertically-stacked silicon nanowires MOSFETs (SNWTs) were experimentally investigated as one of the possible solutions to achieve both high speed, low power consumption in combination with high integration capabilities for future LSI applications. To evaluate the potentials, analyze and improve the performance of these devices, source/drain series resistance for thick source/drain region were studied. Carrier transport mechanisms and the controllability of threshold voltage for vertically-stacked SNWTs with separated gates were also investigated. The influence of in situ doped SEG source/drain was examined for vertically-stacked channel MOSFETs. A large enhancement, by a factor of 2 in the drive current, was obtained when in situ doped SEG process was adopted. Detailed parameter extraction from the electrical measurements showed the RSD values can be reduced by 90 and 75% for n- and p-FETs, respectively, when in situ doped SEG is reinforced by adding ion implantation. On the other hand, by combining the ion implantation to SEG process, VT roll-off characteristics and the effective mobility behavior are slightly degraded. Mobility analysis revealed an increase in the Coulomb scattering with LG scaling, indicating the diffusion of dopant atoms from S/D regions. Further improvements in the performance can be sought by optimizing the S/D activation annealing step. In order to enhance the performance of the vertically-stacked nanowire MOSFETs, the carrier transport limiting components caused by short channel effects were assessed. The optimization of drive currents will have to take into account specific effects to vertically-stacked SNWTs. In particular, the use of SiGe sacrificial layer to make vertically-stacked channels cause large mobility degradation due to the surface roughness, resulted from the damage of plasma etching. This leads to the poor ballisticity in the short channel SNWTs. Hydrogen annealing was shown to be advantageous for improving the surface-roughness limited mobility. Charge pumping measurements, however, revealed that circular-shaped SNWTs, which are formed by annealing, have a higher interface trap density (Dit) than rectangular ones, leading to low-field mobility degradation. This high Dit could be caused by the continuously-varying surface orientation. The resulting additional coulomb scattering could partly explain the quite low mobility in 5 nm diameter SNWTs together with the already known transport limitations in NWs. In addition, the vertically-stacked SNWTs with independent gates by internal spacers between the nanowires to control threshold voltage (named Φ -FETs), were evaluated. Φ -FETs demonstrated excellent VT controllability due to inter-gate coupling effects. Numerical simulations to optimize Φ -FETs structures show that when the spacer width is reduced, the DIBL value can be lowered by a factor of 2 compared to independent-gate FinFETs with the same silicon width. The superior scaling of F-FETs with narrow spacer results from a better electrostatic control which also attenuates the inter-gate coupling. Overall it was shown that using vertical stack structure can increase the drive current density while allowing for better threshold voltage controllability. As for the performance benchmark, nanowires with a diameter of 10 nm, showed the most acceptable balance between mobility, short channel effect. However, to further improve the device performance, process induced surface damage of nanowires must be mitigated.

Milene CLAVEL University of Grenoble

Integration of Transistors with Epitaxial Graphene Channel using a CMOS-based Technology

Graphene consists of a single atoms plane reorganized in honeycomb lattice. Ideal graphene has astonishing properties coming from his electronic band structure in Dirac cone. One of these properties is an exceptional mobility indispensable for future transistors. In this work, properties and performance of transistors based on graphene are evaluated. Sublimation of silicon carbide substrates has been developed to produce state-of-the-art graphene layers and transistors with metal gate and high-k dielectric gate stack and with gate lengths down to 50nm are fabricated using a CMOS-like integration. A study of the impact of annealing steps on transistor performance is carried out and shows that devices with mobilities up to more than 2000cm²/Vs can be fabricated with a channel thickness of about 1nm. We present also in this work a combination of methods developed to enumerate the number of graphene layers obtained on the silicon carbide surface.





Kavita SURANA University of Grenoble

Towards Silicon Quantum Dot Solar Cells: Comparing Morphological Properties and Conduction Phenomena in Si Quantum Dot Single Layers and Multilayers

Quantum confined silicon, in the form of silicon quantum dots of diameters 5 nm or less, has the property of bandgap control and light emission. This bandgap engineering gives silicon quantum dots applications in novel photovoltaic devices, while maintaining compatibility with existing silicon technologies. These dots can help reduce lattice thermalisation losses in a single-junction solar cell. This work focusses on the large scale fabrication of silicon quantum dots in SiO2 using Plasma Enhanced Chemical Vapor Deposition (PECVD), followed by high-temperature annealing. Thick single layers are compared with multilayers for morphological, electrical and optical properties. Devices with these layers are compared with different electrode materials. Film thickness dependent organization of dots is observed in thick single layer structures which demonstrate improved electrical conductivity, but poor optical response. Multilayer films demonstrate augmented and controlled Si bandgaps and improved absorption in the blue-green visible range, accompanied by poor electrical conductivity. The improved optical properties are a promising sign for any potential photovoltaic integration.

Anne-Sophie STRAGIER

University of Lyon

Elaboration and Characterization of Silicon-On-Insulator Structures Made with the Smart Cut™ Technology and Integrating a Thin Embedded Porous Silicon Layer

Double layer transfer of a thin single crystalline Si layer becomes mandatory for a wide range of application (electronic, MEMS, PV). By anodizing a Si substrates, a thin porous layer could be achieved that present the unique properties from one side to be stable at high temperature and from another side to remains mechanically fragile. This work were focused on the elaboration of thin porous Si layer, as well as the characterization of the physical properties of the layer and their evolution under chemical, mechanical and thermal treatment. Thus, the optimal parameters such as the porosity and the thickness were determined to be compatible with mechanical opening with blade insertion. The Smart Cut™ technology was then customized to transfer a thin single crystalline Si layer on substrates comprising a thin porous Si layer on its surface. Such a Silicon On Porous Layer presents the particularity to allow devices processing even at high temperature, and to allow a second transfer after re-bonding and separation in the porous layer. Such a structure and double-transfer technology was demonstrated during these works.

Marie GORISSE

University of Grenoble

Development of RF Devices based on Phononic Crystals

In the straight line of photonic and microwave meta-materials, phononic crystals are foreseen to enable novel acoustic applications that existing technologies cannot reach. These phononic crystals are periodic organization of acoustically different materials exhibiting, for example, stop bands, which means frequency ranges in which no wave can propagate in the structure. In this thesis we target RF frequencies in order to investigate applications complementary to the conventional resonators or filters widely used in mobile telecommunication systems.

We developed a simple process flow to realize micrometric two-dimensional phononic crystals on a piezoelectric membrane. These structures are fabricated along with Lamb wave devices studied in CEA-LETI for channel filtering in low consumption wireless transmission architectures, and with bulk wave resonators or more complex structures like band-pass filters. A parametric study of Lamb wave resonators sharpens our knowledge on these devices, which allow us to design and fabricate delay lines to characterize acoustic transmission properties of phononic crystals.

From a theoretical point of view we set up a simulation model using finite element method. This model was used to design the phononic crystal we realized, and to take into account the effects of the modifications brought by the technological realization. We then fabricated phononic crystals, and electrically and optically characterized them, in collaboration with FEMTO-ST institute. Measurements confirmed the presence of band gaps at the targeted frequency, but over a wider frequency range than predicted by calculation. A detailed study of band diagrams is attributing this phenomenon to the presence of deaf bands, which cannot be excited by interdigitated fingers. This shows that the determination of these deaf bands is of critical importance in designing phononic crystals for practical applications.





Mathieu CUEFF University of Grenoble

Piezoelectric Micro-Actuators

PZT is a piezoelectric material which exhibits very good performances for microsystems actuation. In this work, the problem of sol-gel deposited PZT integration is discussed. First, state of the art of piezoelectric MEMS and PZT is presented. Then, the fabrication of homogeneous (100) and (111) oriented PZT thin films are presented. Layers thicknesses are comprised between 100nm and 2µm. Thirdly, ferroelectric and piezoelectric coefficient was greater than -150 pm/V and the e31,f reaches -16 C/m2. For (111) oriented films, the d31 and e31,f reach -100 pm/V and -14 C/m2 respectively. To explain observed differences, domain walls pinning was studied. Next, fabrication and characterization of a low voltage, fully packaged and thermally stabilized RF MEMS piezoelectric switch is presented. At the off-state, the switch isolation is - 44 dB at 2 GHz. At the on-state, insertion losses are -0.74 dB at 2 GHz. The integration of a metallic gauge in a piezoelectric cantilever is also presented. Finally, developed processes are integrated in membranes fabrication without any degradation. A preliminary reliability study is presented. The failure mechanism of our components is an aging mechanism. This shows that our sol-gel deposition process is well-controlled on 8 inches wafers.

Adam KOSZEWSKI

University of Grenoble

Reliability of Electrostatic MEMS Switches

As MEMS achieve maturity, reliability concerns become of paramount importance. The operating characteristics of electrostatically actuated MEMS (such as RF MEMS switches) are often hampered by dielectric charging effects. As a result this thesis tries to elucidate the physical mechanism and the origin of the dielectric charging in RF MEMS switches, to identify the factors accelerating this phenomenon, how it can be characterized and to study the impact of the properties of the dielectric material on the long term behavior of the fabricated switches. In this thesis two dielectric materials and two switch types are investigated. At first, the structural properties of the dielectrics are characterized in order to detect any deviation in composition of these materials related to the deposition conditions. Secondly, the dielectric properties of these materials are characterized by measurements on MIM-capacitors. The conduction mechanisms are studied by I-V measurements, while the trapping kinetics is determined using a constant current injection technique. Based on these results, we propose an original model which uses the identified conduction mechanisms and the kinetics of charge trapping in the dielectrics to predict the voltage drifts in the investigated MEMS switches under specific operating conditions and, in particular, under a constant voltage stress. It turns out that the model offers a strong potential for a quantitative lifetime prediction. In particular it can be effectively used for screening the potential materials to be used in RF MEMS switches and to investigate the effect of switch design on its long term behavior.

Lionel TENCHINE

University of Grenoble

Getter Effect in Metallic Multi-Layers for MEMS Applications; Elaboration-Microstructure-Behavior Relationship Study

Whilst satisfying low-cost requirements, performances and lifetime of many MEMS can be enhanced by performing wafer-level packaging of devices under vacuum or controlled atmosphere conditions. However, this implies the use of non-evaporable getters (NEG) inside MEMS cavities for residual gases removal. Relationships between elaboration, microstructure and pumping behavior of NEG thin films are investigated in this thesis. After a literature review on MEMS hermetic sealing and getter effect, NEG thin films pumping behavior modification by metallic sub-layers addition is presented. Then, in order to explain this modification, elaboration parameters and thermal treatments influence on thin films microstructure is analyzed. Lastly, nitrogen gettering behavior of NEG is characterized, as well as activation and pumping mechanisms. From these results, some recommendations for NEG thin films integration in MEMS are finally proposed.





Mathieu PY University of Grenoble

Time of Flight Mass Spectrometry: Upon Spatially Resolved, Quantitative Analysis

This work has been devoted to the development of different solutions for improvement of ToF-SIMS analytical abilities to enable accurate quantification of materials and structures for next generation devices. Sample preparation, experimental conditions, data treatment and comparison with other cutting edge characterization techniques have been addressed. We focused on particular materials and structures, namely SiGe or high-k based materials, Ultra Shallow Junctions and materials for organic electronics. In particular we setup an original protocol based on a full spectrum data treatment approach for Ge quantification in strained or relaxed SiGe alloys. The same approach was applied to ultra-thin high-k dielectric materials for sub-32 nm gate stacks. The protocol compares well with data from High resolution Rutherford Backscattering Spectrometry and parallel AR-XPS. We also setup a protocol for backside sample preparation that allows direct access to the bottom of the gate stack for multi-technique analysis (ToF-SIMS, XPS, MEIS). Finally we also worked on organic materials, and especially on PMMA - C60 blends for polymer based resistive memories. We demonstrated the feasibility of quantitative depth profiling of such blends.

Luc MARTIN

INSA Lyon

Advanced Proximity Effects Correction Methods for Direct E-beam Lithography: Application to the Sub-32 nm Node

In electron beam lithography, a new proximity affects correction strategy has been imagined to push the resolution capabilities beyond the limitations of the standard dose modulation. In this work, the proximity affects inherent to e-beam lithography have been studied on the newest e-beam tools available at LETI. First, the limits of the standard dose modulation correction have been evaluated. The influences of each step of the lithographic process have also been analyzed from a theoretical point a view. A simulation approach was built and used to determine the impact of each of these steps on the patterned features. Then, a new writing strategy has been fully developed. It involves sub resolution features known as eRIF (electron Resolution Improvement features) which provide a finer control of the dose profile into the resist. Since the eRIF are exposed a top the nominal features, this new writing strategy is called multiple pass exposure. In this work, the position, the dose and the design of the eRIF have been studied and optimized to get the best of this new strategy. To do so, experiments were led in a clean room environment, and minimization algorithms have been developed. It has been demonstrated that the eRIF provide a significant gain compared to the standard dose modulation. Improvements have been observed even on the most critical levels of the Integrated circuits. By using the multiple pass exposure with optimized eRIF, the resolution capabilities of the e-beam tool have been reduced by 2 technological nodes. The design rules that have been determined to use the eRIF the most efficient way were finally implemented in INSCALE, the new data preparation software developed by ASELTA NANOGRAPHICS. This way, multiple pass exposure can be used in an automated mode to correct full layouts.

Maylis LAVAYSSIERE

University of Grenoble

Electrical and Chemical Mapping of Silicon PN Junctions using Energy-Filtered X-Ray PhotoElectron Emission Microscopy

This thesis addresses the problem of imaging of model systems such as planar silicon pn junctions, fabricated by localized epitaxy, using the novel energy-filtered X-ray PhotoElectron Emission Microscopy (XPEEM). The objective is to improve the understanding of the phenomena influencing the XPEEM images of the junctions, with as long-term perspective, a possible application of this method in a complementary way to existing techniques of 2D dopant mapping. The studies were carried out over three types of junctions realized for this purpose and presenting variable electrical filed (p+/p, n+/p, p+/n). We firstly developed and optimized a three-step surface passivation protocol which yielded a surface close to flat-band conditions. This process allowed us to deduce band alignments as a function of doping level and type on both side of the junction thanks to spectromicroscopy XPEEM imaging of secondary electrons (to determine the work function), Si2p core-level and valence band with both laboratory photon sources and synchrotron excitation. Contrast in core-level imaging due to the first atomic layer of the surface was also shown. Then we highlighted the role of the lateral electric field across the depletion zone of a pn junction which sifts its apparent position in PEEM imaging. We compared experimental results with simulations performed with SIMOIN software to estimate the influence of pn junction properties on PEEM imaging. Dark field imaging of the junction was also simulated. Comparisons with the experimental results showed that it can be used to localize the real junction position.



Core&Beyond CMOS

- CMOS FDSOI Low Power
- Enabling 20nm Fully Depleted SOI Technology
- Strain Engineering in CMOS FDSOI
- Improving the Oxide/Nitride Wet Etching Selectivity to Address the 20nm FDSOI Integration Challenges
- Fully Depleted SiGe pMOSFETs for DualChannel Integration
- Dissipative Quantum Transport in Silicon Nanowires based on Wigner Transport Equation
- Advances in 3D CMOS Sequential Integration
- Low Temperature FDSOI Devices Reach Standard High Temperature Process Performance
- Plasma Immersion Ion Implantation Integration
- Tungsten CMP Process Development for Contacts Levels on Advanced CMOS
- Physically-Based, Multi-Architecture, Analytical Model for Junction-Less Transistors
- Optimization of Ultra-Scaled MOSFET for Single Electronics Applications
- Graphene Transistors with High-k/Metal Gate Stack
- Physics to IC Design for Performance Assessment of Fully Depleted SOI Technologies

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CMOS FDSOI Low Power

Research Topics : Variability on FDSOI

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Sponsorship : CATRENE projects

Partnership : IMEP

The planar Fully-Depleted Silicon-on-Insulator (FDSOI) technology is a powerful architecture for 20nm node and beyond to pursue the CMOS scaling thanks to its outstanding electrostatics and record immunity against variability. Indeed, $A_{\Delta VT}$ performance close to 1mV.µm has been demonstrated, allowing also excellent yield and low voltage operation of SRAM cells.

The variability of the drain current in all regimes has been characterized in order to properly define SPICE models for logic and analog applications. In this study [1], correlations between electrical parameters fluctuations (I_{SAT}, I_{OFF}, SS_{SAT}, V_T, R_{ON}, etc) are presented for 6nm ultra-thin body MOSFETs. They allow discriminating quantitatively the contributions of V_T- and R_{ON}- on I_D-variability. In addition, we have carefully studied the impact of R_{ON}, R_{SD} and V_T on the ON-state current variability thanks to various technological splits: T_{SI}, strained SOI substrate (sSOI) and junction engineering with low temperature (-100°C) C+P co-implants.

Fig.1 shows a better variability of the saturation current ($\sigma\Delta I_{SAT}/I_{SAT}$) for FDSOI than for bulk devices already published in the literature. It confirms the ability of the FDSOI technology to reduce V_T-variations, as well as I_D ones.



Figure 1. Benchmark of the on-state drain current mismatch in FDSOI vs bulk data in the literature.

 I_D variations are found to be highly correlated with both threshold voltage and ON-state resistance fluctuations. Their respective contributions cannot be directly added to capture σI_D because of an advantageous $\Delta V_T/\Delta R_{ON}$ correlation (Fig.2), itself linked to local T_{SI} fluctuations. Taking into account such correlations is of great interest for an accurate definition of spice model corners (inset of Fig.2). Finally, improving the access resistances (R_{SD}) enables to lowering the R_{ON} variability, and consequently improving σI_D .



Figure 2. Correlations between local fluctuations of electrical parameters for nMOS 6nm thin FDSOI devices.

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Research Topics : CMOS

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Partnership : STMicroelectronics, IBM

20nm FDSOI FET integrity is insured by keeping the channel thickness below 6nm. The downscaling of this silicon thickness not only raises specific technological challenges, such as epitaxial growth or implantation but also metrology questions regarding the reliability of the measurements for such thin films.

Need for accurate metrology of the Si thickness [1]

Silicon thickness TSi is the main driver of SOI devices performance and is also the highest-impact technological parameter. It is thus mandatory to accurately access to its value throughout the whole fabrication process. Spectroscopic ellipsometry allows its precise and non-destructive determination as long as silicon optical properties are known thoroughly. We have demonstrated that if they are kept constant, from TSi=12nm to 3nm, the thickness extracted from the ellipsometric spectra deviates from the one calculated within a model where the silicon optical properties are optimized as a function of the thickness. The need for optimized model comes from the fact that the index of refraction is closely related to the band structure which changes significantly when TSi decreases due to quantum effects. As an illustration Fig.1 shows the imaginary part of the dielectric function (¿2) derived from the optimized model parameters. The low energy peak of the spectrum blue shifts significantly when TSi decreases especially below 7nm. This peak attributed to E1, critical point of the silicon band structure, points out that the model has to consider quantum confinement below 7nm in order to provide the best accuracy.



Figure 1. Imaginary part of the dielectric function (ϵ 2) as a function of energy derived from the quantum model for different TSi (thinning step).



Figure 2. Schematic process flow of FDSOI fabrication presenting the challenges associated with the doping of extremely thin silicon films.

Need for epitaxy on ultrathin doped Si [2]

Doping the extension of a transistor before raised source drain growth is appealing because it allows following bulk-like integration and it is expected to induce high junction abruptness. Indeed the ion implantation is done on a well-controlled SOI thickness and the implantation energy is low and therefore the dopants straggle. However the defects created in the SOI by implantation strongly influence subsequent epitaxy quality as summarized in Fig.2. It eventually leads to defective growth with a dramatic decrease of the electrical performance. It is possible to alleviate very efficiently these limitations by depositing a thin nitride layer prior to implantation allowing SOI films as thin as 2nm to be doped as high as 1.5x1015 at.cm-2 while still being able to grow high quality crystalline silicon on top of them.

Performance optimization: design of source and drain implantation [3]

Source and drain implantation conditions are key knobs to tune the device performance. They span the range going from poor linkup resistance (and thus highly resistive transistor) to extension overrun (and thus leaky device). An original three steps and multi species implantation has proven to efficiently boost the performance with up to 25% gain with respect to the previous single implantation scheme without any degradation of the leakages.

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Strain Engineering in CMOS FDSOI

Research Topics : Strain on FDSOI

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Sponsorship : CATRENE projects

Partnership : EECS Department, Berkeley

The Fully Depleted Silicon On Insulator (FDSOI) technology presents major advantages over the standard bulk CMOS one: an improved electrostatic control and a high immunity to local variations (i.e. good mismatch) thanks to its undoped channel. Previous studies have also shown that channel stress can be used to boost the performance. The limits of stress-induced performance enhancement in FDSOI MOSFETs with gate-length and body-thickness scaling have been assessed [1] via both experiments and quantum mechanical simulations.

To provide guidance for optimization of FDSOI stress engineering, the effects of different directional stresses were measured at low levels of stress and simulated for stress levels up 1.6 GPa, see in Fig.1.



Figure 1. (a) Electron and (b) hole mobility enhancement for different induced stress.

Fig.1a shows how the relative change in electron mobility (μ e) varies with the level and direction of stress. μ e is most sensitive to longitudinal stress. Longitudinal compressive stress reduces the hole transport mass and can greatly enhance μ h (Fig.1b). Vertical (<001>) tensile stress changes the heavy hole subband curvature and thereby reduces transport mass.



Figure 2. Simulated (a) electron and (b) hole mobility (solid lines) and relative enhancement (dashed lines) vs. silicon film thickness (tSOI) for different stress components of 1GPa.

Since the body thickness (tSOI) should also be scaled down to maintain good electrostatic integrity, it is important to examine its impact on stress-induced mobility enhancement. For unstrained Si μ e increases slightly as tSOI is reduced below 4.5nm (Fig.2a). In contrast, the hole mobility μ h decreases as tSOI is reduced below 5nm (Fig.2b). The benefit of stress for enhancing μ h is maintained to lower values of tSOI due to the large reduction in hole transport mass under shear stress.

Stress-induced mobility enhancement in FDSOI MOSFETs diminishes with scaling TSOI below 5nm for electrons but not for holes. Anyway, strain finally still boosts the mobility for both electrons and holes at very short gate lengths and film thicknesses [2].

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Improving the Oxide/Nitride Wet Etching Selectivity to Address the 20nm FDSOI Integration Challenges

Research Topics : 20nm FDSOI Integration

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Partnership : CNSE

When it comes to advanced CMOS fabrication, control of any material loss become very important. Reproducing with extreme reliability the same detailed processes between center and edge (on 300mm wafers) is mandatory to achieve good variability requirements: from a wet processing prospective, a low etching rates is usually preferred.

BOE (Buffered Oxide Etch) is a specific chemical mixture featuring HF (hydrofluoric acid) and NH₄F (ammonium fluoride). This is called a buffered solution since HF and F- coexist in their both acid and base formulation. Further, it is also recognized that these two species form active and stable complexes HF₂- and H₂F₂, HF₂- (HF-F- complex) being the main chemical specie involved in the SiO₂ etching mechanism [1]. BOE is available as a commercial solution sold at a given NH₄F/HF ratio ranging from 7/1 to 100/1: typical associated etching rates are 800nm/min and 10nm/min respectively, the highest etching rate being for the smallest ratio X/1. For process control using low etching rate, process teams usually prefer BOE 100/1.

Another way to create specific BOE ratio (from 1/1 to 20/1) is by mixing HF hydrofluoric acid with NH₄OH ammonia base to form NH₄F ammonium fluoride by acid-base reaction. This "blended" BOE is usually prepared at point of use.

$HF + NH_4OH \rightarrow NH_4F + H_2O$

With careful attention given to the volumes, keeping HF in excess allows to create the NH_4F/HF mixture of choice. Solving chemical equations reveals that HF_2 -specie is transiting through an optimum value when a given HF volume is neutralized by a specific NH_4OH volume (Fig.1). Usual optimum appears for BOE around 3/1 ratio (a ratio that is not commercially available at the present time). The low etching rate requirement is then obtained by a significant dilution of such a mixture.

Several blended BOE have been investigated around the specific 3/1 optimum ratio by measuring the etching rates of the typical materials used today in advanced CMOS fabrication: SiO₂ silicon oxide and Si₃N₄ silicon nitride. Etching rates are reported on Fig.2 for a given etching rate, several blended BOE would achieve the etching thickness requirement but the most diluted one will offer the best etching uniformity across the wafer, especially if spray technology is used [1]. Where wet cleaning solution used in high volume manufacturing shows selectivity of 1:1 between thermal oxide and nitride etching, here we demonstrate SiO_2/Si_3N_4 selectivities up to 10:1. It is possible to etch 5nm SiO_2 and limit the undesired nitride loss to 0.5nm during that same wet etching operation (Table 1).



Figure 1. Distribution of fluorinated species as a function of the added NH_4OH volume to 100cc HF 49% diluted in 1800cc DI: the HF2- species transit through an optimum value around 110cc NH_4OH added.



Figure 2. Thermal oxide etching rates observed for various blended BOE, obtained by mixing specific NH_4OH and HF volumes: etching-rates below 0,1nm/sec can be achieved.

Table 1. Etching rate and selectivity between thermal oxide and nitride for a specific blended BOE, as an example: 30cc HF 49% + 30cc NH₄OH +1600cc DI water.

Materials	Etching rate (nm/min)	Ratio vs. Thermal oxide	
Thermal SiO ₂	7	1	
Nitride Si ₃ N ₄	0,7	10	

BOE can be a relevant option to replace standard HF since it offers higher SiO_2/Si_3N_4 etching selectivity. The low cost requirement is achieved by blending two cheap chemistries: HF and NH₄OH [2].

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Fully Depleted SiGe pMOSFETs for DualChannel Integration

Research Topics : CMOS FDSOI Low Power

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Sponsorship : CATRENE projects

Partnership : STMicroelectronics, IBM

SiGe channels are known to enable to tune the threshold voltage (V_{th}) of bulk pMOSFETs (and to boost the hole mobility μ_h). The SiGe pFET-Si nFET DualChannel (DC) integration leads to symmetrical low V_{th} CMOS with a single Gate stack (Metal & High-K). However few studies reported the integration of (c-)SiGe layer in the channel of Fully Depleted pMOSFETs. All of them were based on thick Si_{cap}/SiGe/Si or Si_{cap}/SiGe stacks on insulator (t>20-30nm). Quantifying the V_{th,p} shift (and the SiGe induced hole mobility gain) is still to be achieved in the case of ultrathin film integration (t_{body}<8nm), as required by device electrostatics control (SCE, DIBL) for ultra-short gate lengths (L<30nm).

We investigate here in the frame of Ultra-Thin Film DualChannel CMOS integration the interest of Si_{0.8}Ge_{0.2}/SOI channel (t_{body}=7.8nm) FD pMOSFETs (with High-K & Metal Gate) combined with Si_{0.7}Ge_{0.3} or Si_{0.7}Ge_{0.3}:B RSD (Fig.1) [1]. We analyse the electrical performances (V_{th,p}, G_m, μ_h , I_{sat}...) as function of gate length (down to 23nm) in order to quantify the relative contribution of Si_{0.8}Ge_{0.2} channel and Si_{0.7}Ge_{0.3} RSD (w.r.t. FDSOI reference).

Epitaxial processes [2]: A dichlorosilane+germane chemistry was used (after a "HF-last" wet cleaning and a low temperature H₂ bake) to grow at 650°C, 20Torr the ~3nm thick Si_{0.8}Ge_{0.2} compressively strained channel, which was subsequently capped by very thin Si layers (~2nm). After gate stack definition, a heavily chlorinated chemistry (i.e. SiH₂Cl₂+GeH₄+B₂H₆+HCl) was used to selectively grow the in-situ boron doped (~2x1020cm-3) Si_{0.7}Ge_{0.3} raised source-drain (RSD), also at 650°C, 20Torr.



Figure 1. Left) High Angle Annular Dark Field STEM picture of a 30nm gate length B'' pMOSFET ($Si_{cap}/c-Si_{0.8}Ge_{0.2}/SOI$ stack with slightly embedded $Si_{0.7}Ge_{0.3}$:B RSD). Right) High Resolution TEM picture of the channel highlighting the atoms in the Si_{cap} , c- $Si_{0.8}Ge_{0.2}$ and bottom Si layers.

 $I_{D}(V_{G})$ measurements of Si and Si_{0.8}Ge_{0.2} channels pMOSFETs (Fig.2-a) show the $V_{th,p}$ shift induced by c-Si_{0.8}Ge_{0.2} (-+ 120mV). This $V_{th,p}$ tuning is due to c-Si_{0.8}Ge_{0.2} Valence and Conduction Bands modification (VB:+200meV, CB:+49meV). From Fig.2-b), one can note that i) the $V_{th,p}$ shift remains constant down to 23nm gate lengths and ii) the c-Si_{0.8}Ge_{0.2} channel

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Figure 2. a) $I_D(V_G)$ measurements of 23nm gate length FD pMOSFETs on SOI and c-Si_{0.8}Ge_{0.2}/SOI (with identical Si_{0.7}Ge_{0.3} RSD). b) Impact of gate length on the threshold voltage of FD pFETs on SOI and c-Si_{0.8}Ge_{0.2}/SOI (W=80nm). c) split table.

The very first variability analysis of SiGe MOSFETs shows that the introduction of SiGe in the channel of FDSOI pMOSFETs does not degrade the pelgrom plots and the A_{Vt} performance (A_{Vt}=1.47mV. μ m, in line with FDSOI best published data).

The split CV mobility analysis indicates that the long channel mobility behavior is governed by the channel material. c-Si_{0.8}Ge_{0.2}/SOI B' & B'' exhibit similar μ gain (+40%) w.r.t. to SOI A & A' (whatever the RSD material, Si or Si_{0.7}Ge_{0.3}(:B)). In order to investigate the physical origins of the transconductance gains, we have extracted the access resistance and low field mobility, μ_0 . Very low R_{access} (1100hm.µm) benefit from Si_{0.7}Ge_{0.3}:B RSD (-60% vs. Si ref), and μ_0 gain larger than +320% is demonstrated at 23nm L_G.

		Α	Α'	B '	B "
long	I _{sat}	1 (ref)		2.1	
channel	strain	r-Si channel		c-Si _{0.8} Ge _{0.2} +	
short channel	I _{sat}	1 (ref)	1.5	2.1	3.2
	strain	r-Si	c-Si	cSiGe	cSiGe
			+	++	+++
RSD		Si	Si _{0.7} Ge _{0.3}		Si _{0.7} Ge _{0.3} :B

Figure 3. Summary of the channel strain levels for long & short pMOSFETs highlighting the correlation with I_{SAT} gains.

Finally, the V_{th,p} shift, the excellent $R_{access} \& \mu_0$ yield together improved saturation current densities, with large I_{SAT} gains in agreement with the Si & SiGe channels strain levels (Fig.3).



Dissipative Quantum Transport in Silicon Nanowires based on Wigner Transport Equation

Research Topics : Modeling of Transport in Semiconductor Nanostructures

S. BARRAUD

This study comes within the framework of prospective research in silicon microelectronics, which tries to take advantage of some phenomena emerging from nanoscale dimensions to continue the downscaling of MOSFET devices. Among the proposed architectures for the future technological nodes, the silicon nanowires (SiNWs) have become an intensive research area over the past years. Then, reliable and rigorous theoretical tools must be developed to model the physics of electronics transport and study the electrical performances of these devices.

We intend to introduce a direct solution approach of the Wigner transport equation (WTE) for investigating quantum transport in SiNWs accounting for both phonon and surface-roughness interactions. The strong analogy between Wigner and Boltzmann formalisms allows to include easily scattering effects by using the same collision operator. It is a real advantage as compared to NEGF method for which dissipative effects are still computationally very challenging. The quantum transport is computed by solving the coupled 3D Poisson - 2D Schrödinger equations by a mode-space approach with the 1D WTE along the source-drain direction [1]. For each energy subband resulting from the mode-space decomposition, the Wigner transport equation can be solved to extract both the electron density and the drain current. The electrical characteristics IDS-VGS calculated in the ballistic regime at VDS=0.01V are shown in Fig.1. An example of Wigner's function resulting from the solution of the Liouville equation is shown in Fig.2. In the highly doped source/drain extensions, a Maxwell-Boltzmann distribution function is recovered. However, in the channel, oscillations of Wigner's function induced by the non-local potential are clearly observed.



Figure 1. IDS-VGS characteristics calculated in the ballistic regime with Lg=15nm and square cross-section varying from 5nm×5nm down to 3nm×3nm.





These oscillations characterize quantum interference effect and clearly demonstrate that this approach can successfully handle all quantum effects.

To go further into the electronic transport description, the scattering mechanisms (phonon and surfaceroughness scattering) are accounted for using the Boltzmann collision operator. The acoustic phonon (AP) and surface-roughness (SR) scattering rates are described in each slice of the NW along the transport direction. Following the self-consistent solution of the 3D Poisson and 2D Schrödinger equations, the scattering rates are updated at every iteration. Fig.3 shows the IDS-VDS characteristics calculated in the ballistic regime and by using the Boltzmann collision operator. It can be observed that the SR scattering is not predominant as compared to the AP scattering. The drain current reduction corresponding to each scattering mechanism can be determined. An IDS reduction of 38% is observed due to the electronphonon scattering for VGS=0.2V and VDS=0.3V, against 9% for the surface-roughness scattering [2].



Figure 3. IDS-VDS characteristics calculated in the ballistic regime and using the Boltzmann collision operator for including the collision term.

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Research Topics : 3D Sequential Integration

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Partnership : STMicroelectronics, IBM

3D sequential integration offers the possibility to use the third-dimension potential and eases the co integration of highly heterogeneous technologies compared to a planar scheme: two stacked layers can be connected at the transistor scale. This contrasts with 3D parallel integration, which is limited to connecting blocks of a few thousand transistors.

However, its implementation faces the challenge of being able to process a high performance top transistor at low temperature in order to preserve the bottom FET from any degradation, as the stacked FETs are fabricated sequentially.

Leti has acquired a high level experience in 3D sequential integration. A synthesis of its work has been presented in an invited paper at IEDM 2011 [1]: the smallest transistors in a 3D sequential integration (gate length= 50nm) has been reported (Fig.1).



Figure 1. TEM cross section of stacked transistors with $\mbox{Lg=50nm}.$

Leti's demonstrations stand out from previous demonstrations by the integration of technological choices suitable to target high performance devices for advanced nodes. In particular, the use of wafer bonding (Fig.2) enables to obtain a top semiconductor channel with perfect crystalline quality and thicknesses control. This is a first requirement to target same performance for bottom and top transistors.

Salicidation is mandatory for advanced nodes devices: still its stability with the top FET process is an issue. The development of Ni based stable salicide (thanks to the incorporation of Pt together with F & W implantation) as well as the development of a low temperature process (<650°C) for top FET fabrication enable its integration (cf. Fig.3).



Figure 2. (a) SEM cross section of a thin Si layer stacked above a transistor layer (b) Infrared and (c) acoustic characterization of bonded top active layer on bottom layer showing full transfer and no bonding defects for 200mm wafer (d) Wafer bonding flow.



Figure 3. Development of a salicide adapted for 3D sequential integration (stable up to 650° C).

The key choices to reduce the top FET thermal budget are the replacement of standard thermal dopant activation $(1050^{\circ}C)$ thanks to the use of Solid Phase Epitaxy at 650°C and high-k dielectrics as gate oxide.

Recently, we have demonstrated that the transistors processed at low temperature reach the performance of standard high temperature processed devices [2].

We developed the key technologies to achieving 3D sequential integration: 1- Molecular bonding to obtain pristine quality top active layer, 2- Solid Phase Epitaxy activation, to match the performance of top FET, processed at low temperature (600°C), with the bottom FET devices, 3- A stable salicide enabling to retain bottom performance after top FET processing. Thanks to its ability to offer fine-grain circuit partitioning at the transistor scale, 3D sequential integration opens up a new field of applications and design [1]. It enables both increasing the density and performances without resorting to aggressive scaling.

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Low temperature FDSOI Devices Reach Standard High Temperature Process Performance

Research Topics : FDSOI Devices, 3D Sequential Integration

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Partnership : STMicroelectronics, IBM

Low temperature (<650°C) process is expected to offer the benefits of decreasing gate stack equivalent oxide thickness (EOT), better work function control and shallower junctions, with respect to standard high temperature process (≈ 1000 °C). Also, for 3D sequential integration, low temperature process is needed to preserve bottom FET performance.

To reduce the thermal budget of the transistor, we replace High Temperature (HT) spike anneal (1050°C) for dopant activation by a Low Temperature (LT) Solid Phase Epitaxy step at 600°C. In this technique, the dopant activation occurs during the recrystallization of an amorphized silicon layer leading to high activation levels. However, the drawback of this technique is the creation of End Of Range (EOR) defects below the initial amorphous-crystalline (a-c) interface. These defects are known to increase the leakage current if they are located in or close to depletion regions.

Another challenge of LT process is the smaller diffusion which can lead to highly resistive access compared to the HT reference.

This year, we have demonstrated that these two issues can be solved on FDSOI devices with thin channel [1] (device cross section is shown in Fig.1).



Figure 1. Cross-sectional X-TEM image of a FDSOI nFET with physical gate length LG=25nm. Channel thickness is 6nm.

Indeed we observe in Fig.2 that the LT devices reach similar $I_{\text{ON}}\text{-}I_{\text{OFF}}$ performance than its HT counterparts. This means that proper implantation conditions have been found to counterbalance the smaller diffusion of LT devices.



Figure 2. Comparison of $I_{\text{ON}}\text{-}I_{\text{OFF}}$ trade-off for planar n- and p-FETS with low and high temperature dopant activation anneal.

This aspect is also confirmed by the equivalent evolution of the subthreshold swing versus gate length as shown in Fig.3a. Another remarkable advance is that we observe no junction leakage increase for the LT devices [2]. This is different from our previous results on 25 nm silicon film FDSOI where we have reported a 1.5 decades higher IDmin current in LT devices in comparison with HT ones, see Fig.3b.



Figure 3. (a) Subthreshold swing (SS) versus L_G roll-off for HT/LT n FETs. (b) Normalized I_{Dmin} median values from statistical measurement of LT/HT nFETs with T_{Si} of 25/6nm.

These results are explained by the lower EOR defects concentrations in or close to depletion regions when the film thickness is reduced.

This work shows that low temperature activation enables to match high temperature process performance for FDSOI devices with thin channel (<10nm).

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Research Topics : Ion Implantation Doping

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Sponsorship : OSEO-ISI

Partnership : Ion Beam Services

Heavily-doped and ultra-shallow junctions are required for continued scaling (sub-32 nm) of CMOS devices. Plasma Immersion Ion Implantation (PIII) or Plasma Doping (PD) processes with our new facility PULSION® offers an alternative and attractive way of doping semiconductors with very low energy ions, high doses and high throughput production. In this context, the LETI ion implantation group is studying several aspects required for the integration of PD processing in fully depleted CMOS transistors built on Silicon-On-Insulator (SOI) substrates with extremely thin (sub-10 nm) top Si layers [1].

We have shown, for example, that optimized experimental parameters have to be determined to avoid the detrimental effects induced by surface charging, guaranteeing then the compatibility of PULSION® with patterned structures [2].

The interplay between ion doses and energies has also been shown to impact directly on the thickness of the amorphous layers created by dopant implantation. This parameter is of fundamental importance since a minimum of 2 nm-thick crystalline layers must be preserved to allow the thermal recrystallization of the amorphous region. Typically, the thickness of the amorphous layers obtained by the PULSION® implantation processes developed in the LETI is 15-25% thinner than those obtained from equivalent implantations performed in conventional Beam Line (BL).

We have as well found the optimal PULSION® implantation parameters to allow similar growth rates of Si overlayer, by Selective Epitaxial Growth (SEG) on both N-type and P-type doped regions [3,4] (see Fig.1). A limiting parameter of the maximum doses that can be used to dope Silicon wafers using PULSION® was identified in this study. Too high doses result in reduced rate of SEG and much defective layers.

With this, we have demonstrated that provided optimum conditions, PULSION® is well-adapted to the realization of CMOS transistors on SOI for sub-32nm nodes.



Figure 1. Growth rate as a function of implantation dose for PULSION[®] (BF3 and B2H6) and Beam Line (BF2+ and B+) implantation (P-Type). In function of the implanted dose the epitaxial layer can be mono-crystalline (1), mono-crystalline with stacking faults and twins (2) or non-existent (3).

In parallel, we explore the advantage of PIII over BL ion implantation in performing conformal implantations, to integrate plasma doping processes in the flow chart of tri-gate devices.

Finally, the PULSION® properties are investigated to develop disrupting concepts for new applications of surface engineering by ion implantation. A combination of different parameters as pressure in the chamber, ions nature and energy, gas flow and pulse configuration, strongly impacts on the process and may result on etching or deposition on the substrate during PULSION® implantation.

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Tungsten CMP Process Development for Contacts Levels on Advanced CMOS

Research Topics : Core & Beyond CMOS

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Partnership : STMicroelectronics

As it allows good local and global planarity of wafer surfaces, chemical-mechanical polishing (CMP) is currently the main processing method in the fabrication of integrated circuits to made multi-levels of metal interconnections. In the course to miniaturization, going to smaller dimensions for CMOS nodes <28nm or new PCRAM [1], the tungsten (W) contacts density >20% becomes the main challenge in terms of topography through dishing and erosion, and recess well controlled by the process performances (Fig.1).

CM Planarization: planarize surfaces / controlled recess



Figure 1. CMP impact on W contact.

The process variables that a CMP process engineer dispose in order to optimize polishing process performance are essentially mechanical in nature: rotational velocities, pressures, particle concentration (by slurry dilution). Modern polishing tools use floating retainer ring in order to contain and position wafers under the carrier during CMP process so in order to boost pad temperature one can play on retainer ring pressure to increase ring/pad friction (Fig.2).



Figure 2. Polishing pressures schema.

So the main CMP concept is to drive the mechanical effect by using the membrane pressure, but the chemical effect is here activated through temperature variation by retaining ring pressure (Fig.3).



Figure 3. (left) With polishing removal rate and $T^{\circ}C$ versus retaining ring pressure and (right) the chemical activation energy through the Arrhenius curve.

The dielectric removal rate remains linear with the mechanical effect and it is well known by the Prestonian relation RR=kPV where P is the membrane pressure, V the wafer velocity from the pad and k the Preston coefficient with all other parameters as consumables and of course T°C.

The impact of the 2 polishing pressure on patterned wafers was carefully studied and summarized on the 2 following graphs (Fig.4).



Figure 4. Dishing and erosion versus membrane pressure at constant ring = 6,5psi.

With a high retaining ring pressure at 6,5 psi the chemical impact on W removal is high. At lower membrane pressure the linear mechanical removal rate is also low and a large dishing is obtained at the lowest pressure 1 psi. The best topography result is obtained at 2 psi and at the 3psi the mechanical effect increase again the erosion on dense patterning. The same behavior is also seen on W contact and the W recess can be adjusted (Fig.5).



Figure 5. W contact recess controlled by pressures.

We demonstrate therefore that just by tuning <u>Pressures</u> we can balance the CMP process from more <u>Chemical</u> to more <u>Mechanical action</u>, adjust W/TEOS selectivity and therefore, control W and TEOS lines depth [2]. This highly influences the erosion and dishing evolution, but also influences post-CMP W surfaces quality.

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Physically-Based, Multi-Architecture, Analytical Model for Junction-less Transistors

Research Topics : Analytical Model for Transport in Junction-Less MOSFET

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Sponsorship : FP7-SQWIRE

Partnership : Tyndall National Institute

The Junctionless Transistor (JLT) concept has been recently proposed as a possible candidate for the continuation of Moore's law down to very small gate length [1]. The JLT is a simple N⁺ or P⁺ Si nanowire resistor. A Tri-Gate MOSFET architecture can be used to electrostatically pinch-off (deplete) the central part of the device to turn it off. In the on-state, the silicon is in a flat-band regime and behaves as a simple resistor. The principle of the device requires neither junctions nor any doping concentration gradients between the source, the channel and the drain. The key to fabricate a junctionless gated resistor is the formation of a semiconductor layer that is thin and narrow enough to allow full depletion of carriers when the device is turned off. The semiconductor also needs to be heavily doped to allow a decent amount of current flow when the device is turned on. The actual electrical performances of such devices are not fully understood. Then, the development of a physicallybased analytical model, validated with TCAD simulation, has been developed to predict both the performance and the scalability of JLT. In this work, the usual assumptions used in previous analytical models for investigating transport in junctionless devices are revisited. A new first-order model is then derived to describe the pinch-off ($V_{\text{po}})$ and flat-band (V_{fb}) voltage and the drain current [2].



Figure 1. (top) Comparison between TCAD simulation (symbol) and abrupt depletion approximation model (solid line). (bottom) Relative error between abrupt model and TCAD and between our model and TCAD, showing an overall better agreement, especially for thin films. T_{si} =6,12,25nm, T_{ox} =1nm, N=2×10¹⁹cm⁻³.

The determination of V_{po} is inspired from the solution of Poisson-Boltzmann equations in thin film. The calculation of the flat-band voltage needs to take into account the degeneracy due to the high doping levels that are required in this device. It is based on the metal gate workfunction, the bandgap and electron affinity depending on the doping level. Then, the variation of the depletion region with the gate voltage is described by using an empirical expression, with a power-law variation between the pinch-off voltage (V_{po}) and the flat-band voltage (V_{fb}) . This new description enables to easily address multiple MOSFET architectures, and retains the most important feature: a gradual opening of the channel above V_{po} , up to V_{fb} . Contrary to the usual analytical models based on a "abrupt depletion approximation", our model show a better agreement with TCAD simulation (Fig.1). Indeed, TCAD simulations show that the usual abrupt depletion approximation is not entirely suitable for very small films. Finally, V_{po} and V_{fb} being determined, the drain current can be calculated. This model has been used to calculate the drain current in planar and double-gate JLT by keeping a constant $V_{po}=0.5V$. The I_{ON} current is calculated at $\bar{V}_{GS} \mbox{=} 1 \mbox{V}$ and $V_{DS} \mbox{=} 1 \mbox{V}.$ In Fig.2, we see that keeping V_{po} constant actually does not increase the I_{ON} current with increasing the doping (red color in Fig.2). We can observe that the thickness required to keep a constant V_{po} needs to strongly reduce the silicon film down to 5nm and below. A comparison with TCAD simulation has been performed for Tsi=10nm. A good agreement is observed for both planar and double-gate JLT. Further study in more advanced modeling (quantum corrections, short-channel-effects) is under investigation.



Figure 2. I_{ON} current (V_{GS} =1V, V_{DS} =1V), T_{ox} =1nm, metal workfunction 5.2 eV. For Planar and DG geometry (Width 1µm, L_G =1µm). Symbols are corresponding TCAD simulations.

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Optimization of Ultra-Scaled MOSFET for Single Electronics Applications

Research Topics : Beyond CMOS

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Sponsorship : FP7-AFSID, ANR-POESI

Partnership : INAC

Single electronics effects are today highlighted because of their acknowledged potential for addressing ultra-low power applications. To design device showing Single Electron Transistor like behavior, *ie* a conductance showing oscillations as a function of the gate voltage, it is mandatory to create a confined potential within the device. We show here how the behavior of a standard Si MOSFET can be turned into Single Electronics behavior by tuning some of its technological features.

Dopant induced confinement



Figure 1. 4K vs. 300K FDSOI MOSFET behavior pointing out a isolated dopant induced resonance.

In a first approach we have shown that single dopant located in the middle of a MOSFET channel can induce well behaved resonances in the G(V) characteristic when the temperature is cooled down. These results are obtained on ultra-scaled ($L_G = 10$ nm) devices, enabling high coupling of the dopant to the Source/Drain. In Fig.1, from [1], three sharp dopant peaks are observed. These dopants are well-centered in the channel as is manifested by their high conductance. Therefore they substantially impact the subthreshold leakage in the device at room temperature leading to reduction of VT in comparison to device without centered dopant (not shown here).

Schottky barrier defined SET

Another way to create barriers to induce non monotonic behavior is to design Schottky barriers. Temperature spectra of a pMOSFET (see Fig.2) show different regimes depending on whether thermo-ionic emission (high T) or tunneling (low T) is the dominant transport mechanism. The interesting point is that when temperature is cooled down to 4K the confinement induced by the Schottly barriers is strong enough to induce Single Electron features in the drain current [2].



Figure 2. Temperature evolution of a Id(Vg) curve of a large (W=500nm) Schottky MOSFET.

Back gate tuned barriers

Finally taking advantage of the unique back gate of FDSOI device a dual mode device behaving either as a field-effect transistor (FET) or a single electron transistor (SET) has been fabricated. Depending on the back gate polarization, an electron island is accumulated under the front gate of the device (SET regime), or a field-effect transistor is obtained by pinching off a bottom channel with a negative front gate voltage, as illustrated on Fig.3.



Figure 3. Both SET and FET operations can be achieved with a single device while tuning the temperature and the backbias.

These studies are lead in collaboration with CEA research institute in Nanoscience and Cryogeny (INAC), and are supported by European and French programs.

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Graphene Transistors with High-k / Metal Gate Stack

Research Topics : Beyond CMOS, Graphene, Carbon Electronics

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Sponsorship : FP7-GRAND, ANR-XPGraphene, Carnot Funding

Partnership : IMEP-LAHC, INAC

Since its discovery in 2004, graphene, a one atom thick layer of carbon, is a new rising material in microelectronics. Graphene features excellent properties, such as a huge intrinsic saturation velocity (108cm/s) and the highest measured carrier mobility (200 000 cm²/V.s for suspended graphene). Recent work on epitaxial graphene grown on SiC substrate offers large scale integration opportunities with conventional top-down lithography. Graphene covers the entire surface of the SiC substrate and high quality sheets of few layers graphene can be obtained. Because of the absence of band gap in graphene is an issue, logic applications are not the prior target for graphene. However, thanks to its huge carrier mobility, graphene enables transistors to operate at very high frequency, and cut-off frequencies up to 170GHz have already been demonstrated.

In this work, graphene layers were obtained using the thermal decomposition of the Si-face of hexagonal Silicon Carbide (SiC) in vacuum at 1400°C during 1 hour. The annealing process had been optimized to obtain homogeneous graphene on the entire surface of the wafer and also to guarantee a really low surface roughness after graphitization [1]. TEM microscopy (Fig.1) was employed to estimate the number of graphene layers, indicating the presence of three to four layers of graphene. Fig.2 shows the Raman spectra, the G and 2D peaks being the signature of graphene.



Figure 1. TEM cross-section of few layers of graphene obtained by decomposition of SiC.

Graphene devices were then fabricated directly on the SiC substrate [2]. The first step consisted in patterning graphene into nanoribbons with width down to 50nm. Then, a high-k dielectric was deposited on the entire surface of the substrate. For the metal gate, a stack of 20nm of titanium and 100nm of gold was thermally evaporated and patterned with a lift-off process. Source/drain electrode areas were then opened through the high-k layer, and the source/drain electrodes were made of 20nm nickel and 100nm of gold with a lift-off process.



Figure 2. Raman spectra of SiC and graphenized SiC samples.

The electrical characteristics of the device, measured at 20K before any annealing, exhibit a small modulation of the drain current by the gate voltage, with an lon/loff ratio of 1.5. We do not expect a large modulation since 2D graphene features no bandgap, and 100nm wide graphene ribbons are expected to feature a negligible bandgap of a few meV. To improve the performance of the device, the sample was annealed at 230°C during one hour in nitrogen in order to remove impurities located on the graphene layers. After the annealing, the lon/loff ratio is improved up to four and a maximal transconductance of 140µS/µm is measured which corresponds to a field effect mobility of 50 cm²/V.s. A higher annealing at 300°C during 1h significantly improves the performance of the device. As shown in Fig.3, outstanding current densities are obtained, with a maximal Gm that reaches now 5000 μ S/ μ m at VD=3V and a field effect mobility equal to 2230 cm²/V.s.



Figure 3. Transfer characteristics and transconductance of a graphene transistor after a 300°C / 1 hour annealing under neutral atmosphere.

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Annual Research Report 2011 Silicon Technologies & Components

Physics to IC Design for Performance Assessment of Fully Depleted SOI Technologies

Research Topics : CMOS FDSOI Low Power

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Sponsorship : CATRENE projects

Partnership : STMicroelectronics, IBM, IM2NP, IEMN, IMEP LAHC

Since few years, significant issues as the increase of the device complexity, variability, circuit heating and difficulties to improve the integration density appear in the development of advanced CMOS technology nodes. These trends generate an important growth in development and production costs. Simulation and modeling are also becoming promising tools to quantify the relevance of the new device architectures and to support technological developments and process optimization. At Leti, we estimate the performances and the power consumption before and during the process optimization of advanced CMOS SOI technology nodes thanks to Integrated Circuit simulations. For this, advanced physical tools are developed to expand our physical knowledge. This enables us to improve and adapt TCAD commercial tools to advanced nodes. Moreover, we also develop analytical and SPICE models [1] that mainly use TCAD data as input for the establishment of predictive model cards (Fig. 1).



Figure 1. Strategy for circuit performance assessment.

Advanced simulation is focused on the calculation of the carrier mobility in FDSOI, tri-gate, and nanowire architectures. Mobility is governed by quantum confinement of the inversion layer. 1D and 2D Schrödinger/Poisson solvers are developed and the main scattering mechanisms are considered: electronphonon, oxide/silicon interface roughness, and remote Coulomb scattering. The mobility is then implemented in analytical current models, which are validated using advanced device simulations [2] (Fig. 2).

TCAD process and device simulations are validated on experimental data as illustrated in Figure 3 where simulation correctly describes the ground plane doping profile and the back bias impact in the case of Ultra-Thin BOX FDSOI technology. TCAD mobility model describing phonon, surface roughness and remote coulomb scattering limited mobility in accordance with experimental data is used. Impact of quantum confinement and thin film layer is also taken into account. Moreover, for projections, we resort to analytical models achieved from physical simulations.



Figure 2. Validation on an analytical model for the reflexion coefficient in a silicon nanowire, using advanced Wigner quantum transport simulations [2].



Figure 3. Example of validation of TCAD process and device simulations on Ultra-Thin BOX FDSOI technology.

Finally, the performance and power consumption analyses are obtained from IC simulations using SPICE models specifically developed for advanced technologies. For example, UTSOI model is a SPICE model dedicated for FDSOI technologies [1]. The model parameters are adjusted from electrical data provided by TCAD process and device simulations for more accurate prediction. Including process integration aspects, we have virtually optimized FDSOI MOS transistors for the 28nm and 20nm nodes. It is highlight by figure 4 where the frequency of a ring oscillator is simulated for these both nodes and compared with bulk technologies.



Figure 4. Evaluation of circuit performances in regards to technology nodes.

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Memories

- Scalability of Split-Gate Charge Trap Memories Down to 20nm for Low-Power Embedded Applications
- OX-RRAM
- Phase Change Memories Challenges: Materials and Processes Solutions
- Germanium or Tellurium Rich GexTe1-x for PCM: an Overview on Electrical Characteristics
- PCM as Synapse for Ultra-Dense Neuromorphic Systems: Application to Complex Visual Pattern Extraction
- Resistive Memories: Simulation of Emerging Technologies for Innovative Design Solutions



Scalability of Split-Gate Charge Trap Memories Down to 20nm for Low-Power Embedded Applications

Research Topics : Memories, Embedded Memories, Charge Trap Memories

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Sponsorship : CATRENE-REFINED

Partnership : IMEP LAHC CNRS

Due to the increasing demand for consumer, industrial and automotive products, highly reliable, and low integration cost embedded memories are more and more required. In this context, split-gate charge trap memories were proposed for microcontroller products, combining robustness to defects, scalability, and low power consumption.

Split-gate charge trap memories were processed in LETI with a "memory last" configuration, meaning that the Memory Gate (MG) is deposited on the Select Gate (SG) electrode. Electron beam lithography was used to define control gates down to 40nm. The electrical memory gate length is controlled by the poly-Si layer overlapping the memory channel (Fig.1), allowing to achieve gate length down to 20nm. Various gate stacks were integrated with Si-nc or Si3N4 charge trapping layers.

The split-gate memories are programmed using Source Side Injection, biasing both the memory gate and the source electrode at high voltages. The select gate potential is set in order to operate close to the threshold regime (IS~10µA). Fig.2 shows the program characteristics of a Si3N4 split-gate memory, for various programming VMG and VS, demonstrating ~4V of memory window. Various erasing modes were used depending on the nature of the charge trapping layer: (1) nitride based memories are erased using Hot Hole Injection (HHI), (2) Si-nc memories with HTO control dielectrics are erased by Fowler-Nordheim (FN) injection through the top oxide. HHI allows faster erasing speed but suffer from a higher current consumption. Si-ncs split-gate memories presented a good retention behavior, with >2.5V of memory window after 10 years at 150°C, suitable for automotive embedded products.

A study of the impact of the memory gate length scalability was performed, putting in evidence the enhancement of the memory window for the shortest devices. This behavior was explained by TCAD simulations, and attributed to electrostatic phenomena appearing in short channels. Fig.3 shows the programming window and corresponding energy consumption for various LGM. Indeed, the gain in programming speed demonstrated previously in small devices allows a clear energy consumption reduction (<1nJ required for sub-40nm devices), promising for contactless embedded applications.



Figure 1. SEM plane view (a), schematic (b) and TEM (c) cross section of a split-gate charge trap memory.



Figure 2. Programming (left) and erasing (right) characteristics of a split-gate memory employing Silicon nitride (Si3N4) as a charge trapping layer.



Figure 3. (top) Programming window of Si3N4 split-gate memory for various memory gate lengths as a function of the programming time;. (bottom) measured programming consumption energy.

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OX-RRAM

Research Topics : Resistive RAM

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Sponsorship : CARNOT Funding	Partnership : LTM, STMicroelectronics, Nanyar
	University, IM2NP, DISMI, Sapienza, IHP, IMI

RRAM is an emerging non-volatile memory technology candidate to overcome the intrinsic scaling limitation that standard Flash technology is experiencing. In particular RRAM devices based on binary metal oxide, as HfO2, are particularly interesting because of their ease of fabrication and high promising performances in terms of low operating voltages, high commutation speed and BEOL compatibility.

The working principle of the device relies on its capability to switch between two different resistance levels, after a preliminary one-time process called "forming" which activated the reversible switching. The latter is achieved by applying the proper polarization on the metallic electrodes that sandwiches the active material.

The proper choice of the electrode materials are known to play a crucial but still unclear role in determining the electrical performances of the cell. Moreover the forming process, which requires a higher voltage, poses serious issues to the technology success.

We conclusively clarified the impact of Ti electrodes on the electrical behavior of HfO2-based RRAM devices. To this aim, devices with Pt, TiN and Ti electrodes were fabricated (see Fig.1a-b) and characterized.



Figure 1. (left) Schematic of the integrated devices. Interfacial layer (IL) arises from the O-getter character of Ti. (right) HRTEM image of active stack on device S2.

Ti was found responsible of bipolar switching activation and more importantly it strongly reduces forming (Fig.2) and switching voltages with respect to Pt-Pt devices with a further beneficial contribution to variability reduction (Fig.3). Eventually, it positively impacts on retention.



Figure 2. Forming voltages for analyzed splits. Ti presence reduces forming voltage.



Figure 3. Write voltage for different operating speed on S1 (Pt-Pt) and S4 (TiN-Ti). Ti reduces both voltage and its variability.

To support and interpret our results we have performed several physicochemical measurements, electrical characterization, ab-initio calculations and modeling. We have, for instance, investigated the origins of the resistivity change during the forming of HfO2 based RRAM using TEM, XPS and AES. These studies show that several Hf oxidation states coexist in the HfO2 layer after forming (see Fig.4) which confirms that oxygen plays a major role in this process [2].



Figure 4. (a) Top: SEM image of the HfO2 surface after the local forming. Bottom: Plot of the spectra intensity of C KLL, O KLL and Hf MNN Auger electrons (b) Derivative of the signal intensity of the H MNN Auger electrons as a function of their kinetic energy.

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Phase Change Memories Challenges: Materials and Processes Solutions

Research Topics : Materials, Integration

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Sponsorship : MEDEA +, Nanosciences Foundation

Partnership : STMicroelectronics, ASM, Grenoble INP, CNRS, University of Liège

Phase change memories (PCMs) are nonvolatile memories based on the unique property of some phase change materials, such as GeTe and Ge2Sb2Te5, (GST) to be able to quickly and reversibly switch between an amorphous and a crystalline state that are characterized by very different resistivity values. It is worth noting that in depth understanding of material properties is still missing and specific issues can be solved by materials and process improvement. Key results have been obtained this year concerning the two following aspects:

(i) To allow these memories to operate under relatively high temperatures, it is crucial to improve the stability of the amorphous phase in order to increase the retention time.

(ii) High electrical current is required to reset the information. It has been demonstrated that energies can be highly decreased by reduction of the active volume and confinement of the phase change material. To do so, phase change materials deposition route with high filling capacity is needed.

Concerning retention, using temperature and time resolved resistivity measurements, we investigate the stability of amorphous GeTe doped with C [1]: the activation energies of crystallization of amorphous GeTeC4% and GeTeC10% are about a factor two higher than the GeTe one. This suggests that C doped GeTe could provide both good data retention (related to amorphous stability) and also good programming performances (related to crystallization velocity).

In order to understand this behavior, in depth analysis of material structures were conducted [2]. By combining x-ray total scattering experiments and ab initio molecular dynamics, we show that carbon deeply modifies the structure of the amorphous phase through long carbon chains and tetrahedral and triangular units centered on carbon. A clear signature of these units is the appearance of an additional interatomic distance, around 3.3A in the measured pair distribution function (cf. Fig.1).

Regarding reduction of RESET current, we work on the challenging development and integration of Atomic Layer Deposition (ALD) processes.



Figure 1. (a) Measured structure factors S(Q) for undoped and carbon-doped amorphous GeTe. (b) Measured and calculated pair distribution functions g(r). The measured curves are shifted vertically by 3.

The obtained ALD GST layers present the targeted composition, a nice uniformity on 200 mm wafers, a low roughness, a high conformity and a classical phase change behavior. As expected, the resistivity variation between the as deposited amorphous layer and the crystalline structure is of 4 orders of magnitude.

Finally, these films were successfully integrated in pillar PCM cells. The cell switching between low resistive and high resistive state was obtained during 106 cycles without degradation as shown in Fig.2.

This work demonstrates the feasibility of Phase Change Memory cells using GST deposited by ALD at industrial scale.



Figure 2. Endurance of PCM devices using GST deposited by ALD. The PCM cell is written and erased under RESET (100ns, 4.8V) and SET (1200ns, 2.4V) conditions, respectively.

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Germanium or Tellurium Rich GexTe1-x for PCM: an Overview on Electrical Characteristics

Research Topics : Phase-Change Memories, GeTe Chalcogenide Materials

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Sponsorship : CATRENE-REFINED

Partnership : STMicroelectronics

Phase-Change Memory (PCM) is widely recognized as one of the most promising next-generation non-volatile memory technologies and a present valuable alternative to the Flash mainstream [1]. Main advantages are low voltages, fast read/write, good scalability and low cost. PCM is based on the of electrothermal-induced phase transition а chalcogenide alloy between an amorphous highresistance state (named RESET) and a polycrystalline low-resistance one (SET). Very old studies at material level focused on GeTe as candidate for optical storage. The stoichiometric composition exhibits very fast crystallization behavior, while departing from the 50:50 composition the alloys become very slow, because material segregation is suspected.

We have employed these materials in solid state PCM memories and investigated the features of such host material in the electrical domain.

Program (SET)/erase (RESET) characteristics were collected with different SET pulse widths. Ge30Te70based devices need long SET pulses (in the order of microseconds) to show a recrystallization of the active phase change area (in agreement with results obtained by optical tests). The long crystallization time might be correlated with the expected phase separation of Te and the formation of the compound GeTe, requiring a slow diffusion process. Despite the low speed, this stoichiometry shows the lowest RESET current density (of about 50 MA/cm2).

TABLE II PROGRAMMING PULSE PARAMETERS

Device	SET Current	RESET Current	Min SET Time Width	SET Power	RESET Power
	[MA	cm ²]	[ns]	[MW	//cm ²]
Ge30 Te70	26	51	3000	7.1	65.1
Ge40 Te60	14	60	50	3.4	79.2
Ge50 Te50	10	68	50	3.3	87.7

The high speed of the crystallization for the other two stoichiometries (50 and 60 at % Te devices) is highlighted by the low resistance reached with the shorter SET pulse of 50 ns. A synoptic table on all results concerning programming characteristics is reported above.

The results of the endurance test confirm the high resistive contrast between the RESET and the SET states for all the three stoichiometries. The test conditions (e.g. pulse intensity and duration) were selected in order to obtain the largest programming window. In Fig.1, we report the endurance test for Ge40Te60 device. Note that all the GexTe1-x-based cells showed the possibility to obtain a very good endurance up to more than 10^7 cycles not shown here.



Figure 1. Endurance test for Ge40Te60-based device. The RESET pulse width is 50 ns; the SET pulse width is 500 ns.

In data retention experiments the failure criterion considered, is the reaching of a resistance equal to half of the initial RESET state that stands for the loss of the state of information. The extrapolated fail temperature for ten years shows the expected improvement of the PCM cell data retention by increasing the Te content in the chalcogenide material. A high activation energy is reached by 70 and 60 at. % Te devices (Table below).

TABLE III DATA RETENTION RESULTS

Device	Extracted Activation Energy	Extrapolated Fail Temperature for 10 years
Ge30Te70	$3.6\pm0.1~\mathrm{eV}$	$126 \pm 1^{\circ}C$
Ge40 Te60	$3.1\pm0.2~{\rm eV}$	$117 \pm 4^{\circ}C$
Ge50Te50	$2.2\pm0.2~{\rm eV}$	$95 \pm 7^{\circ}C$

By all these results, Ge40Te60 compound seems to be a good compromise between speed, power consumption, endurance and data retention performances, making this alloy a good candidate for embedded applications.

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PCM as Synapse for Ultra-Dense Neuromorphic Systems: Application to Complex Visual Pattern Extraction

Research Topics : Phase-Change Memories, Synapse, Neuromorphic Circuits

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Sponsorship : CATRENE-REFINED

Partnership : CEA-LIST

The development of biologically inspired neuromorphic circuits, in order to achieve low power, highly parallel, and fault-tolerant systems, has gained a lot of interest over the last few years. Still there lies а considerable gap between the fields of semiconductor devices, computational neuroscience and system-design before a fully functional large scale hardware neuromorphic system will be realized. We choose PCM technology because of the advantages it offers compared to the other resistive memory technologies, such as maturity, scaling capability, high endurance, and good reliability.



Figure 1. Illustration of biological synapse and concept of using PCM as synapse in neural circuits.

Fig.1 shows the biological synapse and the basic concept of emulating it with PCM. An electronic device emulating the biological synapse should be able to gradually increase (long term potentiation, LTP) or decrease (long term depression, LTD) its conductance in response to neuron spikes. To demonstrate these features, lance-type PCM test devices, with a 100nm-thick phase change layer and 300nm-diameter tungsten plug, were fabricated and characterized.

We propose a new energy efficient synapse circuit consisting of two identical PCM devices ("The 2-PCM synapse") with a realistic and simplified programming pulse scheme, represented in Fig.2. One PCM device (LTP) has a positive current contribution, while the other PCM device (LTD) contributes negatively towards the output CMOS neuron current. In the "2-PCM synapse", crystallizing the LTP PCM device produces synaptic LTP-like effect, while crystallizing the LTD PCM device produces synaptic LTD-like effect. Since gradual crystallization can be obtained by applying simple identical pulses our approach simplifies the pulse schemes for implementing learning in large scale neuromorphic systems.



Figure 2. Circuit schematic of the "2-PCM synapse".

Address-Event Representation (AER) data (Fig.3) recorded with 128x128 pixel silicon retina was used as the input for our PCM neural network. The goal of the neural network is to detect cars passing in different lanes on a freeway in an unsupervised way.



Figure 3. AER dataset for pattern recognition. Represents 6 car lanes.

With our approach we were able to emulate a spiking neural network with about 4 million synapses, capable of complex visual pattern extraction with an average detection rate of 92%, and a system power consumption of 112μ W for learning.

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Annual Research Report 2011 Silicon Technologies & Components

Resistive Memories: Simulation of Emerging Technologies for Innovative Design Solutions

Research Topics : PCRAM, CBRAM, OXRAM

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Sponsorship : CARNOT Funding

Partnership : STMicroelectronics, Altis, ISEP, IM2NP

Simulation and modeling activities have been realized in collaboration to Silicon divisions' technologists and in the frame of several projects relative to Phase Change Random Access Memories (PCRAM), Conductive Bridge Random Access Memories (CBRAM) and Oxide Based Random Access Memories (OXRAM).

PCRAM, CBRAM and OXRAM belong to the emerging field of resistance switching memories.

PCRAM operation relies on the fast and reversible switching between the amorphous and crystalline phases of chalcogenide materials (such as GST) which exhibit very different electrical conductivities. The TCAD simulation activity follows two main objectives:

- Development of in-house simulation software [1] with a realistic crystallization model based on the Level Set Method. This tool provides an insight on crystallization mechanisms: nucleation or growth dominated (Fig.1).
- ii) A material screening study based on Design of Simulations to understand the influence of material properties on the reset current.



Figure 1. Visualisation of the phases during a crystallization pulse (blue: crystal, green: high resistivity amorphous phase, orange: low resistivity amorphous phase, brown: melted).

Unipolar OxRRAM resistive switching can be explained by the creation/dissolution of a metallic filament. A compact model developed at IM2NP [2] allows for evaluating the performances of this new technology in FPGA applications [3]. Table 1 shows the gain in area and time compared to Flash and PCRAM technologies. In both cases, the gain is significant particularly with the current market solution of Flash memories in the configuration of an FPGA. Table 1. Performance evaluation for OxRRAM technology (2x2 switchbox) [2]

	Cell elements	Area (F ²)	Write time (ns) [13]
SRAM	72T	2576	2.4
Flash cell	48T	1104	24000
PCM cell	8T24R	321	1440
OxRRAM cell	8T24R	229	84
Flash vs. OxRRAM	-	x4.82	x285.7
PCM vs. OxRRAM	-	x1.4	x17.14

CBRAM switching relies on the formation/dissolution of a Silver rich conductive filament which shunts the top and the bottom electrodes through a solid electrolyte such as GeS_2 for the devices developed in the LETI-ALTIS collaboration framework. The simulation activity includes:

 Ab initio simulations to understand the thermodissolution of Silver in electrolyte (GeS2) - in order to mimic both dissolution and retention phenomenon



Figure 2. GeS2/Ag before and after thermo-dissolution from a molecular dynamic simulation.

 ii) 1D laws are derived in order to take into account both the thermally activated diffusion and its enhancement due to an electric field effect; a physical compact model for performance evaluation is under development.

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Patterning

- IMAGINE : Development of Resist Process Solutions
- IMAGINE : Development of Maskless Lithography
- 193 Lithography Negative Tone Process for 20 nm Technology
- Block Copolymers Directed Self Assembly for CMOS Application



IMAGINE : Development of Resist Process Solutions

Research Topics : Lithography

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Sponsorship : TSMC, ST, SOKUDO, ASELTA, MENTOR Graphics, SYNOPSYS

Partnership : MAPPER lithography, TOK, JSR, DOW EM, NISSAN Chemical

With the resist partner of the IMAGINE program [1], TOK - JSR - DOW EM - NISSAN Chemical, CEA-LETI pursued its work on process development for the low energy multibeam lithography developed by the Dutch company MAPPER Lithography BV.

During 2011, more than 50 advanced formulations provided by resist partners have been prepared and tested at LETI. The key objective is to push the resolution capability of Chemically Amplified resist. For the performance of this work, all direct write E-Beam lithography capabilities of CEA-LETI have been employed. Resist pre-screening has been performed at 50keV on the latest platform developed by VISTEC, VSN3054DW. Then, to push resolution capability, VISTEC VB6 UHR Gaussian beam platform operated at 100kV and with sub-10nm spotsize has been used. Finally, most promising platforms have been tested on the MAPPER multibeam platform. All process optimizations have been jointly performed with SOKUDO on the 300mm RF³ track.

	escreening (Advanced screening	MAPPER multibeam
LETI	VISTEC	VISTEC	MAPPER
TOOLS	SB-3054DW	UHR VB6	ASTERIX S004
VOLTAGE	50 kV	100 kV	5 kV
TYPE	Shaped Beam	1 Gaussian beam	110 Gaussian beams
CURRENT	[0.1 - 512] nA	[0.1-10] nA	0.07nA/beam
Spot size	Eq. to CD pattern [~20 to 1600] nm	~10 nm	Today~20-25nm
Wafer size	300mm	200mm	300mm
ACTIVITY	-50:50 R&D and Production (full wafer)	-50:50 R&D and Production	100% R&D

Figure 1. CEA-LETI EBDW lithography capabilities.

The first axis on process development work is dedicated to the optimization of the technological stack. Taking benefit of low energy concept, the trilayer stack strategy, including spin-on-carbon material, spin-on silicon hardmask and imaging resist has been selected to reduce the backscattered effects and therefore enhance image contrast [2]. This choice also presents the key advantage to be widely used and known in CMOS production lines.



Figure 2. Imaging performance comparison on reference stack and silicon.

Among the new formulations tested at CEA-LETI, several platforms showed 20nm hp resolution capability at 100kV. Those platforms tested at 5kV reached 24nm hp resolution on the MAPPER tool with 25nm spot size, aligning the capability of this technology for the 16nm logic node. This resolution limit is even expected to be improved with the implementation of the new projection optics with smaller spot size characteristics.

	28nmhp L&S 50kV VSB	20nmhp L&S 100kV Gaussian 10 nm spot size	24nmhp L&S 5kV MAPPER 25nm spot size
<u>RESIST B</u>			
<u>RESIST A</u>			

Figure 3. Best resolution.

End of 2011, significant progress has been achieved on resist platform development. Chemically amplified resists have been pushed below 20nm half pitch capability gaining in 1 year close to 10nm resolution. To pursue further resolution capabilities and deal with roughness and pattern collapse concerns, CEA-LETI enlarged end 2011 its R&D activities. The impact of underlayer, developer and post rinse treatment is also under investigations. 1st results have been already published. The work axis will be intensified in 2012 [3].

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IMAGINE : Development of Maskless Lithography

Research Topics : Lithography

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Sponsorship : TSMC, ST, SOKUDO, ASELTA, MENTOR Graphics, SYNOPSYS, TOK, JSR, DOW EM, NISSAN Chemical

Partnership : MAPPER Lithography

In the latest ITRS roadmap, Maskless remains as one of the candidate to address lithography needs for the sub-16nm technology nodes. Considering the problems and delays with extreme ultraviolet (EUV) lithography — and the costs of multi-patterning — multi-beam is worth exploring. Maskless lithography makes sense for prototyping or small-lot production, where it could potentially eliminate the masks' cost.

Starting July 2009, LETI and MAPPER have initiated the open collaborative program IMAGINE [1] focused on the assessment of the MAPPER technology. A first 110 beams pre-alpha has been installed.





Figure 1. MAPPER pre-alpha platform in LETI.

This tool follows a pretty aggressive ugpgrade program to qualify each key components related to the basic concepts of this technology: (a) Blanking system, for multibeam addressing in raster scan mode, (b) Stage control and displacement for stitching performance (below 15nm in a first step), (c) Projection Optic System (POS), for ultra-high resolution capability (below 22nm spot size), (d) Monitoring to qualify the tool status and the overall reliability. Following performances have been shown:

• The blanking system has been installed since 2 years and 95% of the beam are in spec. No degradation has been observed on process latitude and resolution at 32nm half-pitch and below.

• The stage positioning system has been improved by adding an interferometer system along the exposure direction. This upgrade has demonstrated beam to beam stitching concept allowing exposure within $3x50\mu m^2$ field size with less than 15nm of stitch error [2].



Figure 2. 45nm contact exposed with 2 neighbouring beam.

• The POS upgrade extends resolution capability to 22nm



Figure 3. Best resolution achieved in CAR for line/space and contact.

• One of the first concerns regarding tool performance is the overall reliability. The aim of the tool assessment is to know the key parameters: current per beam, spot size, etc, to get a confident metrology in order to qualify the lithography capability. A weekly monitoring of the tool versus the exposure conditions has been carried out providing the first control chart for statistical process control (SPC) data. This follow-up activity allows tracking of the key parameters to make the next generation machine improvements.



Figure 4. Correlation between beamlet spot size (pink data) with 32nm CD (blue data). Positif drift of spot size showing POS aging.

End of 2011, the tool is configured with 110 beams driven individually and can resolve 22nm hp features in positive tone chemically amplified resist. This achievement confirms the potential of this technology to address CMOS manufacturing. The IMAGINE program with its industrial partners will continue its assessment mission in 2012 and will pursue the gualification of the new planned upgrades on the LETI platform: beam to neighbouring stitching, allowing 20x200µm² field size, and alignment demonstration. The reliability studies with SPC analysis will be further to demonstrate the correlation between the lithography results, CD and CDu, versus the key tool parameters. Then the next beta-tool platform, MATRIX, with a throughput capability of one wafer per hour, full field 300mm, will be delivered end of 2013.

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193 Lithography Negative Tone Process for 20nm Technology

Research Topics : Lithography

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Partnership : STMicroelectronics, Resist Suppliers

One way to push down the limits of 193nm immersion optical lithography is to address the Metal and Vias levels with Negative Tone Development (NTD).

CEA-LETI is developing NTD process to provide a lithography solution to its device R&D program focused on the 20nm logic node.

NTD Principles

NTD technology consists in exposing a 193nm positive resist and to develop the un-exposed resist area with an organic solvent (on the contrary of standard acidobasic development where exposed resist area are dissolved). The interest of such process resides into the better optical contrast which is obtained from a brightfield mask instead of a darkfield mask, which allows obtaining trenches and contact holes with a better resolution than with a classical ArF lithography process [1].



Figure 1. Schematic comparison of NTD technology with standard optical lithography process.

NTD process performances

This process installation has been started in Q4 2010 with SOKUDO support. It is now developed in two 300mm tracks at LETI. The major difficulties reside firstly in optimizing development recipes in units not dedicated to this type of process, and secondly in the evaluation and the compatibility of several specific NTD resists and developers newly developed.

The technical feasibility of NTD process has been demonstrated at 45nm CD (Pitch128nm) Trench and 90nm dense contact holes (Pitch 180nm) with very good uniformity using a dry ArF scanner (NA=0.85) in collaboration with our partners resist suppliers.

These results and the minimum critical dimensions obtained, 30nm for trenches and 60nm for contact holes, meet the expectations of our industrial partners including STMicroelectronics for 20nm nodes and beyond.



Figure 2. Snapshot and intra-wafer CD uniformity of trenches and contact holes obtained using NTD process.

NTD process stability

Because NTD requires specific development modules, current R&D configuration study for NTD qualification is made in stand-alone mode. The purpose of this work was to evaluate the impact of PEB-Development delay time on lithography performances.

Several parameters have been tested as PAB and PEB temperature, developer, underlayer type and resist intrinsic parameters (quencher, polymer and activation energy) [2]. A stabilisation could be obtained after 24h whereas the CD reduction in the first hour remains whatever the process condition used. So it is important to take this impact into account in production environment.



Figure 3. Post-exposure delay time investigation: CD reduction versus PEB-development waiting time.

Finally this NTD process paves the way for the realization of new integrations to meet the needs of Metal and Via levels. The combination of this process NTD with double exposure technology appears very promising to achieve the very advanced technology nodes.

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Block Copolymers Directed Self Assembly for CMOS Application

Research Topics : Self-Organization, Self-Assembly, Block Copolymers

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Sponsorship : ANR PNANO, ENIAC-LENS

Partnership : LTM/CNRS, ARKEMA, LCPO

Density multiplication of patterned templates by directed self-assembly (DSA) of block copolymers stands out as a promising alternative to overcome the limitation of conventional lithography. Self-assembling materials used in conjunction with the most advanced exposure tools may enable extension of current manufacturing practices to dimensions of 10 nm and less.



Figure 1. a) Schematic view and b-d) associated CD-SEM images of graphoepitaxy approach with film thickness.

For directing self-assembly process, several groups including our own use an artificial topographic surface pattern generated by "conventional" lithography. This approach is called "graphoepitaxy". We show this year that a long range order can be generated by increasing the polymer film thickness with respect to guiding pattern height, with the best results obtained for a BCP film thickness higher than the trench depth (see Fig.1).

Moreover, a customize software was implemented in LETI (see Fig.2). Based on Delaunay triangulation, this methodology allows us to qualify and quantify defects in order to ensure the DSA process robustness.



Figure 2. a) Initial image (by CD SEM) b) the image after defect identification; in blue no defect, in red and yellow defects [3].

Thus, we propose a methodology to optimize the guiding lithography patterns in order to improve the long range order of the block copolymer patterns. Zero-defects configurations are generated when commensurability of L0 (copolymer intrinsic period) is respected for both the line width L and the space width S. (see Fig.3).



Figure 3. Zero-defects unidirectional network generated when commensurability is respected.

These results show the high potential of DSA to be integrated directly into the conventional CMOS lithography process in order to achieve high resolution and pattern density multiplication, at a low cost and point out the necessity of a 300mm baseline. Preliminary studies engaged in LETI show no major issue concerning the integration of PS-b-PMMA selfassembly towards 300mm CMOS requirements

Based on these promising results, LETI and ARKEMA have initiated this year an open collaborative program focused on material development and their associated process implementation for nano-structuring by DSA.

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Power Electronics & Photovoltaics

- Power Electronics
- Film Thickness Dependent Conduction in Ordered Si Quantum Dot Superlattices
- ZnO Nanowires Sensitization with Different Absorber Layers
- Integration of Electrodeposited ZnO Layers in Hybrid Polymer Solar Cell
- Si Exfoliation by MeV Proton Implantation
- Heterostructure Deformation and Layer Transfer
- Synthesis of Carbon-Based Materials for Nanoelectronics and Technologies for Energy



Power Electronics

Research Topics : GaN, HEMT Power Transistors

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Partnership : INES, CNRS-LMGP

The goal of this research project is to develop a new generation of GaN power transistors on 200mm silicon substrate. The interest of GaN transistors is the reduction of energy losses and the capability to work at temperatures greater than 200°C, relaxing cooling requirement.

We have developed an efficient 600V HEMT power transistor with a maximum current greater than 100A as illustrated in Fig.1. The first generation of this device is a normally-on transistor with a threshold voltage of V_{th} =-5V. This device is composed by 3 unit devices of 33A in parallel.



Figure 1. GaN HEMT structure.

The main advantage of this transistor is the high electrical conductivity allowing a reduction in the quantity of energy lost. The Id(Vd) curve for one unit device is shown in Fig.2. A 33A drain current is obtained at a drain voltage of V_{ds} =8,5V. To reduce Vds at 2V we plan to multiply the chip area by 4 so that a device of 94mm² will be able to pass 100A at Vds=2V.



Figure 2. Id(Vds) of one 33A transistor unit.

Another advantage of using GaN technology is the higher operating temperature. The maximum working temperature of silicon power device is 150°C, while GaN power transistors show an optimal characteristic up to 200°C. Indeed, the increase of Rdson is less than 17% between 150°C and 200°C (see Fig.3).

Concerning the maximum operating voltage, this first generation GaN device sustains more than 1000V in off state (breakdown voltage at 25°C).

Fig.2 shows a drain leakage current at Vgs=-8V. Part of this leakage is due to the Schottky contact which forms the gate. In order to reduce this leakage, the introduction of a Metal Insulator Semiconductor (MIS) structure for the gate electrode is necessary.



Figure 3. Id(Vd) as a function of operating temperature.

In contrast to silicon, the native oxide of gallium nitride is not a high quality insulator. Therefore this native oxide must be removed, and replaced with a high quality dielectric. Aluminum oxide Al2O3 is one of the best candidates as its conduction band offset is above 2eV and it can be easily deposited by atomic layer deposition (ALD).

Native oxide removal issue has been addressed through chemical and plasma treatments and characterized by X-Ray Photoelectron Spectroscopy (XPS).

As illustrated in Fig.4, the introduction of 10nm of aluminum oxide deposited by ALD reduced the gate current leakage by 2 to 3 orders of magnitude.



Figure 4. Schottky vs MIS Gate leakage currents.

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Annual Research Report 2011 Silicon Technologies & Components

Film Thickness Dependent Conduction in Ordered Si Quantum Dot Superlattices

Research Topics : PV, Nanocrystals Based Heterostructures for PV

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Partnership : INES, CNRS-LMGP

Si based new concepts for solar cells aim to achieve compatibility with current industrial technology, even as they try to increase cell efficiency with novel cell architectures [1]. This has been possible due to strong quantum confinement effects for dots around 5 nm in diameter leading to bandgap widening from the bulk value of 1.1eV. The quantum dots obtained show an ordered formation in thicker films, leading towards a Si-nc 3D-superlattice kind of structure.

Identical SRO layers were deposited on p-Si wafers (5-10 Ω .cm), using PECVD technique with N₂O/SiH₄=4. The SiO_x films were annealed at T>1000°C, resulting in a phase separation phenomenon (Si QDs and SiO₂), followed by a 400°C forming gas annealing to passivate Si-SiO₂ defect states.

Grazing Incidence X-Ray Diffraction measurements (Fig.1A) show crystalline quantum dots. For the 28.4°, using broadening Si (111) peak, the diameter of the dots was estimate with the Scherrer formula. $L_{vol} = \frac{K_{\rm N}}{\Delta 29 \cos 9}$ where L_{vol} is the volume weighted size of

the crystallites, K is the shape factor (taken to be 0.9), λ is the X-ray wavelength (0.154 nm) and $\Delta 2\theta$ (in radians) is the integral breadth of the Bragg peak. The equation has been used with the integral breadth in order to be independent of the shape (Lorentzian or Gaussian) of the peak. Assuming spherical quantum dots, the dot diameter $d = \frac{4L_{vol}}{2}$



Figure 1. A - GIXRD pattern of Si nanocrystals in SiO₂. Mean nanocrystallite sizes as determined by the Scherrer equation give sizes as 4.8nm (Q30), 5.3 nm (Q50) and 5.1 nm (Q75). B - TEM micrographs - (a) 30nm thick film - (b) 50nm thick film - (c,d) 75nm thick film.

Plane-view TEM micrographs are shown in Fig.1B. The formation of Si-ncs dependence of the film thickness is pointed out [2,3]. It varies from randomly ordered distribution in 30nm and 50nm thick films, to ordered superlattice structures in 75nm thick film.

Conductivity versus 1000/T (Fig.2) shows conduction mechanisms, from temperature dependent activation conduction in A (30nm) to temperature independent tunnelling in ordered superlattice in C (75 nm).



Figure 2. A - Conductivity versus 1000/T at low electric field (-1.0 V) between 80K and 300K. The inset shows a linear fit for m=0.5 in Mott's equation for sample Q30 B - C-V measurements at 1MHz show hysteresis broadening under ambient illumination, confirming photocarriers generation from quantum dots. The filled dots=dark data, hollow dots=illumination data.

Dark current-voltage measurements show that the conductivity decreases with increasing thickness as shown in Fig.2. Tunnelling conduction and Mott's equation have been used to describe temperature (T) dependant conductivity (σ) in quantum dot systems: $\sigma(T) \propto \exp\left(\frac{-T_0}{T}\right)^m$.

The value of m determines the conduction phenomena and possible values include (corresponding to direct tunnelling), 0.5 (Nearest Neighbour Hopping, NNH) and 1 (thermionic emission). Si-SiO₂ interface defects have been passivated. Sample Q30, observed to be temperature dependant activation conduction, can be described by NNH. For sample Q50, the temperature dependence is still large for T>200K, but decreases at lower temperatures; it appears to be a mix of activation hopping conduction and temperature independent activation less conduction mechanisms. For sample Q75, no temperature dependence of conductivity is seen, typical for direct tunnelling. Capacitance-voltage measurements were performed on a sample with a semi-transparent AI film and a bus bar to form a metal-insulator-semiconductor (MIS) device (Fig.2B). Rectifying behaviour was seen in dark and illuminated conditions. A clear hysteresis effect was observed, due to photocarrier generation in the Si QD layer and the charging-discharging cycle of the nanocrystals. This memory effect was only observed at 1 MHz frequencies, microsecond time scales which are much larger than timescales of PV phenomena, and should thus not influence PV properties. The conduction mechanism in identically fabricated Si nanocrystals films depends on the spatial organization of the dots, and on the thickness of the While conduction via nanocrystals and film. photocarrier generation is a positive sign for any solar cell applications, the thickness and material quality must be optimized to achieve a balance between both absorption and electrical conduction.

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ZnO Nanowires Sensitization with Different Absorber Layers

Research Topics : Core/Shell Nanostructures (ZnO/CdTe-CdSe, CuInS2, Cu2ZnSnS4)

R. SALAZAR, S. SANCHEZ, C. LEVY-CLEMENT, V. IVANOVA

Sponsorship : Nanosciences Foundation

Partnership: INAC, CNRS

Wide band gap oxide semiconductors have proven to be useful for numerous applications. Among them, zinc oxide (ZnO) has emerged as a potential alternative material to produce nanoscale electronic and optoelectronic devices. Not only due to his unique optical properties: transparency, near-UV emission, high excitonic binding energy (60 meV at RT) and his suitable electric conductivity for good electronic performance in the nano-regime, but also for the flexibility to obtain it in various nanostructures. The most used strategies for fabricating arrays of vertically aligned single-crystal ZnO nanowires and 2D layers include high-temperature and vapour-phase methods. We have optimized the deposition conditions for their electrochemical deposition either galvanostatically or potenstiostatically. Thus prepared ZnO 2D layers and nanowires could be further used as transparent electrodes and applied in: solar cells, water splitting processes, removal of pollutants in water or gas sensors.

The proposed nanowire-version of extremely thin absorber (eta) solar cell, is composed by a thin semiconductor absorber (Eg $\sim 1.1 - 1.8$ eV) sandwiched between transparent electron and hole conductors (n and p-type respectively with Eg > 3 eV). This configuration requires only a few-tens-of-nanometerthick layer of absorbing material to fully absorb the available solar energy radiation. As a consequence of the thinner absorber and the advantageous electrical and optical properties of the nanostructured electrodes, the photogenerated carries can be efficiently collected and transported through the nanowire channels, Fig.1.

Thin

Successive

Sublimation

(SILAR),

obtained

deposition

lavers

conformably deposited on

the ZnO nanowires (NWs)

[1] surface (Fig.2a) by

Absorption and Reaction

electrodeposition (ECD). Using SILAR method, a 25

nm thick nanoparticle-

like shell of CdS

Close

lon

(CSS)

after

cycles

were

Layer

Space

and

was

20

on



Figure 1. Schematic of the nanowire-version eta solar cell [2].

electrodeposited ZnO nanowires, Fig.2b. For the CdTe prepared by the same technique, the deposited layer was about 12-15 nm after 20 SILAR cycles, Fig.2c [2]. Thin layers of CulnS₂ (CIS), Cu₂ZnSnS₄ (CZTS) and CdTe were also prepared by ECD and CSS, respectively [3]. The CdTe layer obtained after 7 min deposition time is about 40 nm thick and is formed by nanoparticles with diameters up to 20 nm, Fig.2d. Electrodeposited CIS

and CZTS films cover the entire NWs after 0.5 C $\rm cm^{-2}$ passed charged density.

The absorber thickness and properties are controlled by the passed deposition charge in ECD, by the number of deposition cycles in SILAR and by the deposition time in CSS. CdTe layers are with high crystallinity and good optical features for short deposition times and higher number of cycles in SILAR, Fig.3.

The absorber materials prepared by roomtemperature solution based methods are with high quality similar to those deposited by vapor phase counterpart. A photovoltaic effect was observed for the solar cells prepared by solution base methods, while up to 2% was achieved with the vapor phase methods. This is greatly encouraging due to the fact that cheap and easy processing methods could potentially find place in the future industrialization.







Figure 3. Absorbance spectra of bare ZnO NW and after sensitization with indicated absorbing layers. The number of SILAR cycles was 40 for CdS and 20 for CdTe. The deposition time for CSS was 7 minutes. Passed charge for CZTS was 0.5 $C.cm^2$.

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Integration of Electrodeposited ZnO Layers in Hybrid Polymer Solar Cell

Research Topics : PV, Hybrid Solar Cells, ZnO Layers, Electrodeposition

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Partnership : INES

Although recent achievements in organic photovoltaic (OPV) technologies the solar cells based on them still do not strongly contribute to the energy supply due to their low energy conversion efficiency and the lack of long term stability. The growing importance of these devices is related with the possibility to prepare them by wet-processes on lightweight flexible substrates, thus being potentially suitable for large-area low cost fabrication. The integration of ZnO layers as electron transporting layer (ETL) leads to an increased efficiency and stability of inverted PSCs. Recently PCEs of more than 4% (but for an active surface area of 0.06 cm²) on glass substrates with an electrodeposited ZnO interlayer have been reported. Nevertheless, it is still challenging to develop polymeric solar cells on flexible substrates with high performance and long term stability on larger area.

The polymeric solar cell used in this study has the following architecture (Fig.1) : glass or polyethylene terephthalate (PET) covered with ITO layer as the base electrode (R=10-15 Ω /sq), an electrodeposited ZnO thin film as ETL; a solution processed Bulk HeteroJunction (BHJ) layer of poly(3-hexylthiophene) (P3HT) and phenyl C61 butyric acid methyl ester (PCBM), and a PEDOT:PSS film as hole transporting layer (HTL), enhancing the ohmic contact between the polymer and Ag evaporated top electrode.



Figure 1. Schema of an inverted polymer hybrid solar cell structure (1), SEM images of an electrodeposited ZnO layers on glass/ITO (2) and PET/ITO (3).

The electrochemical deposition method for ZnO preparation has been chosen because it is environmentally friendly, low cost, large surface scalable process and offers the possibility to easy control the layer properties. In our study the ZnO thin films have been electrodeposited from an aqueous electrolyte containing zinc chloride, potassium chloride and dissolved molecular oxygen. Using this technique thin films with different thicknesses between 50 and 400 nm controlled by the passed charge density during the electrodeposition (form 0.1 to 0.8 C cm⁻²) have been obtained (Fig.1). It is very important to note that the electrodeposited ZnO films exhibit hexagonal wurtzite structure with preferred growth along the c-axis and further annealing process is not required. PSCs with an

electrodeposited ZnO interfacial layer on both studied substrates have been prepared. Best reached power conversion efficiencies of 3.3% for plastic and 3.2% for glass substrate have been obtained (AM1.5, 100 mW cm⁻²) for an active surface area of 0.28 cm² (Table 1).

Table I. Best photovoltaic device performances obtained on glass/ITO and PET/ITO substrates with ZnO interlayers.

Substrat	V _{oc} , mV	J _{sc} , mA cm⁻²	FF, %	PCE, %
Glass/ITO	596	10.7	50.3	3.19
PET/ITO	587	10.3	54.5	3.29

The results of stability measurements of as prepared PSCs on glass/ITO and PET/ITO substrates over 1000 and 500 hours illumination, respectively, are shown on Fig.2. For comparison reference cells with the ZnO ETL prepared by a wet process are shown. The average losses in the PCE are almost unchanged for devices prepared with thick ZnO interlayer and they are around 15% for the other studied devices for both substrates. For the reference PSC a sharp loss of 30% after 100 h illumination and further continuous faster decrease in PCE is observed.



Figure 2. Normalized PCE for PSCs fabricated on glass/ITO and PET/ITO with ZnO ETL electrodeposited with different charge densities under 1000 and 500 hours continuous illumination, respectively.

Inverted polymeric photovoltaic devices based on electrodeposited ZnO electron extracting layer with high efficiency and remarkable good operation stability have been fabricated on glass and plastic substrates [1, 2]. We show that the electrochemical deposition of compact ZnO thin films on both substrates is a very promising technique and could further contribute to decrease the PV technologies cost. We consider that a big advantage of the electrodeposited layers is the fact that they exhibit good crystalline quality and could be further used in the polymeric solar cells without consequent annealing process, a crucial point for the fabrication technology on plastic substrates. This work was presented on the following meetings [3,4].

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Si Exfoliation by MeV Proton Implantation

Research Topics : Smart-Cut Basic Understanding

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Partnership : SOITEC, CEMTHI-CNRS, INAC

Proton implantation in silicon and subsequent annealing are widely used in the Smart CutTM technology to transfer thin layers from a substrate to another. The low implantation energy range involved in this process is usually from a few ten to a few hundred of keV, which enables the separation of up to 2 µm thick layers. New applications in the fields of 3D integration and photovoltaic wafer manufacturing raise the demand for extending this technology to higher energy in order to separate thicker layer from a substrate.

In this work, we have investigated the effect of proton implantation in single crystalline silicon in the 1-3 MeV range which corresponds to a 15-100 μ m range for the hydrogen maximum concentration depth. We have demonstrated that despites a considerably lower hydrogen concentration at Rp, the layer separation is obtained with fluence close to the minimum fluence required for low energy implantation as shown in Fig.1.



Figure 1. 100 μ m thick delaminated film and donor substrate after 3 MeV / 1e17 H+/cm² implantation and subsequent anneal of a Si (100) substrate.

It appears that the fracture propagation in Si and the resulting surface morphology is affected by the substrate orientation.

In Si (111), implantations at 1.5 MeV lead to delamination of the entire surface after annealing for (111) samples with all tested fluences ($>5X10^{16}$ H/cm²). An example of the remaining substrate surface obtained after delamination is shown in Fig.1a. This is in good agreement with the minimum fluence to detach a silicon layer found by previous studies on the topic.

In Si (100), Implantation at 1.5 MeV with fluence of $5x10^{16}$ H/cm² did not display any observable modification before and after thermal annealing. Implantation with fluence of $7x10^{16}$ H/cm² resulted in sample blistering (Fig.2b). So, it appears that a 30 µm thick silicon layer above the implanted area is not stiff enough to prevent blistering in this case. Delamination has been achieved with implantation fluence of $1x10^{17}$ H/cm² for all energies tested in the range of 1 - 3 MeV. The thinnest films that we obtained have thickness of a few tens of micrometers and are therefore highly breakable. However, films obtained after delamination of substrate implanted with 3 MeV are thick enough to be easily handled (Fig.1).



Figure 2. Sample surfaces after implantations at 1.5 MeV – $7x10^{16}$ H/cm² and subsequent annealing (700°C – 10 mn). (a) Fully delaminated (111) Si surface; (b) Blistered (100) Si surface.

Substrates surface aspect was observed with AFM and SEM after delamination. Morphology depends on silicon substrate orientation. No peculiar morphology is to be seen for the (111) orientation (Fig.3a). By contrast, square grains can be observed on the (100) Si surface. This specific appearance has been observed for all (100) Si delaminated sample with grain size being proportional to the implantation energy (Fig.3b and.c). Grains obtained after annealing of a 2 MeV implanted sample are about two times bigger than those obtained with 1.5 MeV implantation. AFM observation confirms the square shape and the increase in grain size with higher implantation energy.



Figure 3. Substrate surface after delamination for implantations (a) in (111) Si at 1.5 MeV - $1x10^{17}$ H/cm², (b) in (100) Si at 1.5 MeV and (c) in (100) Si at 2 MeV- $1x10^{17}$ H/cm².

In conclusion, behaviours of silicon samples implanted with high energy proton and subsequently annealed have been observed. The minimum fluence to obtain delamination or blistering after implantations in the MeV range proves to be slightly higher but of the same order of magnitude as the fluence needed in the keV range. Orientations (100) and (111) have been tested and delamination is achieved with lower fluence in (111) than in (100) Si. Our results suggests that substrate mechanical properties such as the Young's modulus or surface energy play a predominant part in the last steps of crack propagation to detach layer with thickness of tens μ m. Consequently, delamination appear to be favoured in (111) Si compared to (100) Si.

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Research Topics : Innovative Substrate Elaboration

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Partnership : SOITEC

Heterostructures composed by materials with different properties could lead to very interesting and innovative applications. For instance, bonding a silicon wafer onto a fuzzed silica wafer could lead to attractive structures for display applications. Elaboration of heterostructure is thus very interesting but joining two different materials with different physical characteristics could induce different elaboration problem or operating limitation. For instance, if the materials have different thermal expansion coefficients (CTE), stress is induced during any thermal treatment [1]. Using direct bonding to stack the two materials, no gliding can occur after bonding avoiding any stress release. Such a thermal stress can then disturb post processing or even induce a heterostructure breakage. Different techniques, based on a theoretical stress analytical model, have been developed to minimize heterostructure thermal stress for a given anneal.

The analytical simulations are based on Timoshenko plate theory [2] with infinite elastic plates and small deformation assumption. Two wafers are bonded at T_i and annealed to T_f . Their Young Modulus (E_1 , E_2) and their Poisson coefficient (v_1 , v_2) are constants as well as their thermal coefficient (α_1 , α_2). d_1 and d_2 are the wafer thicknesses and the first wafer is placed under the second one with $\alpha_1 < \alpha_2$. Considering a bonded portion, the internal forces (P) and the moments (M) which maintain the structure in equilibrium are represented on Fig.1 (ρ is the curvature radius).



Figure 1. Heterostructure stress model at a temperature $T_f{>}T_i$ with $\alpha 1{<}\alpha 2$ [2].

Following Timoshenko theory, with $m=d_1/d_2$ and $n=E_1^{*}(1-v_2)/(E_2^{*}(1-v_1)=E_1'/E_2')$, we obtain for two wafers:

$$1/\rho = \frac{6(1+m^2)\int_{T_i}^{T_f} (\alpha_1 - \alpha_2) dT}{(d_1 + d_2) (3(m+1)^2 + (m^2 + \frac{1}{mn})(mn+1))}$$

$$\sigma_{1}(z) = \frac{1}{\rho} \left[E_{1}'\left(z - \frac{d_{1}}{2}\right) + \frac{1}{d_{1}} \left(\frac{E_{1}'d_{1}^{3} + E_{2}'d_{2}^{3}}{6(d_{1} + d_{2})}\right) \right]$$
$$\sigma_{2}(z) = \frac{1}{\rho} \left[E_{2}'\left(z - d_{1} - \frac{d_{2}}{2}\right) - \frac{1}{d_{2}} \left(\frac{E_{1}'d_{1}^{3} + E_{2}'d_{2}^{3}}{6(d_{1} + d_{2})}\right) \right]$$

 σ is the plan stress inside each material.

These equation can be extended for several wafers or layers bonded to each other with imposed initial curvature or internal forces during the bonding.

Using these simulations, it is possible to minimize the impact of thermal stress during elaboration processes. For instance, to manage thermally transfer a thin silicon film onto a fuzzed silica wafer using an ion implantation transfer technique, one can minimize the strain relaxation by doing a hot bonding (Fig.2) or a curved bonding.



Figure 2. Splitting simulation at 400°C of a silicon wafer hot bonded onto a fuzzed silica wafer at 350°C.

It is then possible to obtain a thin silicon layer on top of a fuzzed silica wafer after a thermal splitting at 350°C curved bonding (cf. Fig.3a) or with a hot bonding (cf. Fig.3b). This work was presented at [3].



Figure 3. Thermal splitting of a silicon wafer onto a fuzzed silica wafer, a) at 350° C after a 2m curved bonding, b) at 400° C after a 350° C hot bonding.

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Synthesis of Carbon-Based Materials for Nanoelectronics and Technologies for Energy

Research Topics : Carbon Metallization

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Sponsorship : GRENADA, GRAND, GRAFONICS

Partnership : LTM, Néel Institute, ENSIACET, Cologne University

Graphene, discovered in 2004 by A. K. Geim and K. S. Novoselov, is an excellent electronic material, and has been considered as a promising candidate for the post-silicon and post-ITO ages. It has enormous potential in the electronic device community, for example, field-effect transistor, transparent electrode, etc. Despite intense interest and remarkably rapid progress in the field of graphene-related research, there is still a long way to go for the widespread implementation of graphene. It is primarily due to the difficulty of reliably producing high quality samples, especially in a scalable fashion, and of controllably tuning the bandgap of graphene.

We report a simple and quick route to grow graphene on 200mm wafers, in semiconductor-compatible environment by segregation process without any external carbon sources. The whole work has been done at CEA-LETI clean room using microelectroniccompatible equipments. Single to few layers of graphene can be synthetized in controllable way. Polycrystalline thin films of Ni, Cu, Pt and alloys are being investigated for the tailoring and the nanostructuring of graphene.



Figure 1. Graphene synthetized in full 200mm wafer. SEM image of bilayer graphene deposited on Ni surface with the corresponding Raman spectra. Polymer-based transfer is used to stick the graphene on arbitrary substrates (Si, SiO2, quartz and flexible).

The resulted coverage of graphene upon the wafer is highly uniform with over 98% (fully interconnected) of the whole area in polycrystalline nickel. In principle, there is not any limitation on the size of graphene film. The process developed involves a short annealing of few minutes to get full coverage of graphene on 200mm wafer surface. Transparency over 85% and

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sheet resistance in the range of thousands of Ohm/sq is obtained and should be soon optimized.

Moreover, process techniques would allow to nanostructure the graphene synthesis by either control the interaction of graphene and the metal catalyst or by developing

On the other hand, we develop some capabilities toward the synthesis of hybrid structures containing both carbon nanotubes grown epitaxially under few graphene layers. Furthermore, the composite can be grown using catalyst and temperatures compatible with complementary-metal-oxide-semiconductor processing (T < 450 °C).



Figure 2. Result of the CVD growth at 550 °C during 30 min with the formation of hybrid structure. HRTEM image of the CNT/FGL interface. The dotted lines are guides for the eyes to localize the nanotube tip and the FGLs sheet.

It is established that this mechanism is quite general and that it can be expected to occur in a broader range of process conditions and not limited to unique catalyst.

Carbon based materials are investigated with the aim to develop large area preparation to be implemented in real life application (ICT, PV, energy storage).



Annual Research Report 2011 Silicon Technologies & Components



Passive & RF Components

- CVD Nanowires
- Spin Torque Oscillators for Telecom Applications
- Magnetic/Piezoelectric Thin Film Composites
- Integrated Materials For New Radiofrequency Functions On Silicon
- Influence of Deaf Bands on the Transmission of a Hypersonic AIN Phononic Crystal Slab
- Multiple Frequency Solidly Mounted BAW Filters
- RF Oscillators Stabilized by Temperature Compensated LiNbO3/Quartz HBARs
- Film Bulk Acoustic Resonators based on Single Crystal Piezoelectric Thin Films
- Millimeter-Wave Interconnects for Advanced 3D Silicon Interposers



CVD Nanowires

Research Topics : Si Nanowires Growth, Integration in Capacitors

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Sponsorship : Carnot-CAPAFIL

Partnership : CPE Lyon, ETH Zurich, LTM, INAC

Catalysed CVD Nanowires are used to form new type of nanostructured materials and devices. They are particular in the fact that from a catalyst metallic droplet ((generally gold), a Silicon based gas (e.g. SiH4) is decomposed and lead to the growth of Silicon nanowires (cf. scheme Fig.1 top).

These bottom-up grown structures can bring lots of innovations in the microelectronic field thanks to their specific properties. In particular, they allow the possibility to achieve crystalline semiconductor materials independently to substrate, large surface over volume ratio and high aspect ratios.

However, the use of silicon nanowires in the microelectronic industry is nowadays still limited by the lack of fully CMOS compatible process for the nanowire growth. This is mainly due to the fact that gold, the generally used catalyst, is not compatible with some microelectronics requirements. At LETI, we have recently demonstrated that nanowires growth is possible using a CMOS compatible metal (Cu) and temperature (<450°C) [1] (Fig.1 bottom).



Figure 1. (top) Schematic of the classical CVD nanowire growth; (bottom) SEM pictures of CVD nanowires grown from copper catalyst at 425°C on Si/TiN substrate.

This procedure requires the use of a metallic thin film which reduces the control over the nanowire size distribution. To improve the process, new methodologies are required to build nano-catalyst of selected size with narrow dispersion. We demonstrated nanostructured catalysts by using nano-imprint template and thus localization of the nanowires [2]. In parallel, we have studied the use of an organometallic liquid deposition technique to produce copper nanoparticles of selected size (ranging from 3 to 50 nm), depending on the properties of the surface of the substrate used for the preparation of the nanoparticles.

The CMOS compatible nanowire growth was developed for fabricating highly dense capacitance, embedded in interconnects levels, thanks to the large effective surface deployed by an assembly of nanowires. The Si nanowire growth was followed by conformal depositions of first a high-K dielectric material (Al2O3), then a metallic electrode (TiN) [4,5].



Figure 2. Si nanowire after ALD alumina and MOCVD titanium nitride depositions constituting the unit MOS structure [5].

Thousands of these types of capped nanowires are connected in parallel in our capacitance device. Fig.3 shows the C(V) curve of nanowire-based capacitances (blue curve, 18μ F/cm²), compared to reference planar capacitances without nanowire (red curve, less than 1μ F/cm). This large capacitance gain is directly related to the surface deployed by the nanowires. This technology is very promising for fabricating decoupling capacitances (which require very large capacitance densities).



Figure 3. C(V) with nanowired (blue and green) compared to a structure without nanowires (red) [5].

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Spin Torque Oscillators for Telecom Applications

Research Topics: Spintronics, RF Components

M. QUINSAT, (U. EBELS), M.C. CYRILLE

Sponsorship : Carnot Funding , ANR P3N

Partnership : Spintec

Wireless telecommunication transceivers need singlefrequency RF oscillators as frequency reference for the RF signal processing. The state of art of the current technology is a combination of stand-alone high quality low frequency mechanical resonators (e.g. quartz crystals) and integrated high frequency low-guality LC tank-based phase locked loops. This technology has been mature and low cost for several decades but it faces now severe limitations in terms of integration (large chip area), power consumption and multiple frequency standard compatibility. Part of the morethan-Moore mutation of microelectronics, emerging disciplines such Spintronics offers as new nanotechnologies for RF oscillators based on a recently discovered physical phenomenon: the 'spin torque' exerted by a spin-polarized current. The spin torque allows driving a GHz oscillation of the magnetization in a nanosized (< 100 nm) magnetic tunnel junction, which is then converted back to an AC voltage through the magnetoresistance effect. This novel type of current controlled oscillator is of great interest for future telecommunications applications because of its relatively large frequency tuning range (a few GHz), combined with an extremely small size.

The microwave emission of spin torque nanooscillators (STO) based on magnetic tunnel junctions (MTJs) with MgO barriers and CoFeB electrodes is studied. Macrospin simulations were carried out to evaluate the effect of current induced coupling between magnetic layers inside a MTJ based STO comprising a synthetic antiferromagnet fixed layer. It was found that the Spin transfer Torque interaction between magnetic layers leads to the formation of a collective auto-oscillation mode involving the magnetization of both free and fixed layers and resulting into a substantial reduction of the linewidth of the emitted microwave signal. This is result is of importance when considering the synchronization of STOs as a mean to improve RF performances.

The temperature dependence of the emission linewidth of MTJ based STOs has been also investigated experimentally by means of frequency and time resolved detection techniques, which allow the extraction of the emission frequency, emission linewidth and the non-linear parameters [1,2]. The comparison of the experimental results to the linewidth evaluated using analytical models of a nonlinear auto-oscillator confirms this linear dependence and the role of the non-linear parameters for the temperature range covered experimentally.



Figure 1. (a) Schematics of the oscillator configuration (FL refers to the free layer, TL to the top layer of the synthetic antiferromagnet and BL to the bottom layer of the synthetic antiferromagnet). (b) FWHM linewidth 2Df_{tot} as a function of applied field for coupled FL-SAF structures (green) and for single FL (black) for comparison.



Figure 2. (a) Temperature dependence of the FWHM emission linewidth for three different devices: DevA: 85 nm diameter ($\mu_0 H_{app}$ = 61 mT; I/I_c ≈1.4), DevB: 75 nm ($\mu_0 H_{app}$ = 48 mT; I/I_c ≈1.3) and DevC: 62 nm ($\mu_0 H_{app}$ = 65 mT; I/I_c ≈1.4). (b) The amplitude relaxation rate Γ_p (left axis) and the relative ratio r=2 $\pi\Delta f \Gamma_p$ for a bias current of -1.10 mA, i.e, I/I_c ≈1.4, (right axis) for DevA. (c) Log-log plot of the phase noise S_j and amplitude noise S_{dp} at 300K for the DevA.

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Annual Research Report 2011 Silicon Technologies & Components

Magnetic/Piezoelectric Thin Film Composites

Research Topics : RF Components

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Sponsorship : Carnot-MANDARIN

may lead to instantaneous easy axis / hard axis 90° reversal with E-field. Another main feature is a marked change (~90%) of the remanent magnetization with E-field as shown in Fig.2. This scheme is suitable for magnetic tunable microwave devices controlled by E-field.

1.0

1.0

0.5

Partnership : G2ELab



Figure 2. Evolution of the Squareness (Mr/Ms) of the F/PE composites as a function of E-field.

AF/F/PE composites show a different stress-mediated behavior characterized by a controllable rotation of the direction of magnetization in F. This may lead to 180° magnetization switching with a remarkable change of sign on the exchange bias field (H_{ex}) as shown in Fig.3. This second scheme is particularly suitable for hybrid M*E*RAM and smart-magnetometers [3].

E = 3 MV/m

E = -1 MV/m



Figure 3. Change of the magnetic hysteresis loops of the AF/F/PE composite as a function of E-field showing near 180° magnetization rotation.

Magnetoelectricity (i.e. magnetic properties controlled with E-field) is a beneficial long-waited cross-property (Fig.1) which may significantly reduce power consumption in modern electronics (memory, RF circuits and sensors).



Figure 1. Schematic of cross-properties of materials.

There are two competing schemes today: one considering "natural" multiferroics (MF); the other using "artificial" composites to mimic the previous ones. With "natural" MF, the coupling strength is weak and usually observed at low temperature which severely hinders applications. With "artificial" MF, cross-properties can be engineered at room-temperature, putting composites closer to applications.

Most studied "artificial" MF exploit interfacial magnetoelastic coupling of separate magnetic (F) and piezoelectric layers (PE). In order to increase the coupling strength, high magnetostriction (Λ_s) and large piezoelectric constants (d_{31} , d_{33}) are required.

LETI's thin film composites use ultra-soft magnetostrictive FeCoB electrodes combined with PZT [1]. These composites show remarkable improvements in high performance active materials at room temperature. We report magnetoelectric constants (i.e. coupling factor α of 1.65 µs/m and voltage coefficient M_{EH} of 250 V/cm⁻¹ Oe⁻¹), which is 3 orders of magnitude higher than natural "MF" (BiFeO₃) [2].

Additionally, LETI's thin film composites lead to two scenarios depending on whether one considers single uniaxial ferromagnet (F) or unidirectional exchangebiased antiferromagnetic / ferromagnetic (AF/F) materials.

F/PE composites undergo direct competition between stress (σ) and induced uniaxial anisotropy (H_k). This

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Integrated Materials for New Radiofrequency Functions on Silicon

Research Topics : Radio Frequency, Magnetism, Dielectric, Acoustic

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Sponsorship : Carnot-MANDARIN

Partnership : CEA-LITEN, CRHEA, INL, INAC, Spintec, CNRS-XLIM, IETR, CNRS-LabSTIC

Integration of new magnetic and dielectric materials into silicon has opened up numerous prospects for new radiofrequency (RF) applications such as transmitterreceiver miniaturization, agile communications systems, self-tuning sensors, to meet societal challenges, arising in the biomedical, automotive, domotic sectors. The technological challenge that must be met is on a scale matching that of the anticipated scientific and industrial benefits. Among the range of opportunities at hand, the Radiofrequency Components Laboratory, a unit in the Electronics and Information Technology Laboratory (LETI) at CEA, has elected to work - for some 15 years already - on the integration of new magnetic, and dielectric materials.

Nowadays, magnetic thin films - issued from a line that began with magnetic hard disk drive read/write heads - are found in multiple technologies, involving microwave applications - e.g. oscillators making use of spin electronics, planar inductors for mobile phones, or antitheft tagging systems. Such a wide take-up is due to the fact that thin-film engineering now makes it possible to tune the properties of thin films, to match the target application, by developing new materials whether homogenous, or heterogeneous - featuring structures that are exactly controlled, at a scale of just a few nanometers. Currently, LETI, together with the Nanosciences and Cryogenics Institute (INAC) is able to match the state of the art worldwide, in this respect, owing to a strongly multidisciplinary outlook, spanning the entire range from fundamental physics to technological applications, and microwave instrumentation. Having advanced to this stage, in the field of magnetism, researchers yet have to take up a new challenge: that of constructing devices featuring high operating frequencies, and/or "frequency-agile" operation, e.g. variable inductors - a type of component that does not as yet exist. Achieving this entails overcoming constraints related to limited device dimensions, but equally meeting the new requirements set by applications, in terms of frequencies, quality factors, and power consumption.

Dielectric thin films have likewise seen major advances being made. They are found to be peculiarly suitable for the purposes of sensors, or actuators, making use of the piezoelectric effect (see Fig.1), of built-in high-capacitance capacitors, or voltagecontrolled agile components, e.g. variable capacitors: for instance, micros-witches making it possible for a cell phone to switch from one communications standard to another, or variable-focus lenses used in cameras, or built-in detection capabilities for pacemakers... The fabrication of dielectric thin films, at LETI, involves two types of materials, viz. aluminum nitride (AIN), and oxides coming under the perovskite family. For researchers, this sets a twofold challenge. First, the issue they face is one of ensuring enhanced intrinsic qualities, for the material at hand, thus matching the state of the art - a goal that has already been achieved for AIN and lead zirconate titanate (PZT). Second, they must be able to integrate these films, to make them into devices, while preserving the material's qualities.

Moreover, LETI is currently combining magnetism and dielectrics by investigating magnetodielectric thin films, exhibiting the ability to combine high permeability and high permittivity as shown in Fig.1.



Figure 1. Transmission electron microscopy cross section of a composite multiferroic material, consisting of an alternating stack of magnetic electrodes, mainly consisting of FeCo, to ensure high permeability, and dielectric layers made of SrTiO3 perovskite, making for high permittivity.

Whether it be for magnetic, or dielectric thin films, researchers fully understand the requisite of bringing together the various specific materials, components, and systems-oriented disciplines: a meeting of minds that entails suppressing the separations, or even the barriers, that still set apart physicists, and applications designers.

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Influence of Deaf Bands on the Transmission of a Hypersonic AIN Phononic Crystal Slab

Research Topics : Phononic Crystals

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Partnership : FEMTO-ST

Phononic crystals are periodic structures composed of two or more materials. As their optical counterparts, photoninc crystals, they support frequency band gaps where the propagation of elastic waves is prohibited. Therefore, a two dimensional crystal realized in a piezoelectric slab provides a full 3D confinement of waves. CEA-Leti focuses on the use of these structures for the synthesis of advanced RF components. However, before such components come to life, we need to understand mechanisms behind transmission properties of these structures.

We fabricated phononic crystals composed of air holes in a 2µm-thick aluminum nitride (AIN) membrane using a three masks process lead on 200mm silicon wafers [1]. With a period of 6.6µm and a hole diameter of 4µm, a theoretical stop of 60MHz is expected around 800MHz. This crystal is inserted into a Lamb wave delay-line, as illustrated in Fig.1.



Figure 1. Principle of the phononic crystal delay line: (a) optical photograph and (b) SEM photograph of the phononic crystal.

These delay lines have been measured using a vector network analyzer connected to coplanar RF probes. In Fig.2, we plot the comparison between reference delay lines (blue dashed curves) and delay lines in which the phononic crystal has been introduced (red solid curves). Clearly, the crystal causes a reduction of the transmission signal between 600 and 900 MHz, i.e. over a frequency range much larger than the theoretical stop-band.

This work demonstrates that focusing only on the stop band properties of crystals is not enough for real life application development. Indeed, theoretical transmission calculation reproduces the transmission spectra of Fig.2 [2]. Further investigation reveal that another phenomenon has been generally overlooked in the literature: the coupling efficiency of incident waves into modes of the crystal defines the transmission behavior outside the stop band. Indeed, from the band diagrams of Fig.3, we determined that from 600 to 900MHz, most modes cannot be efficiently excited using Lamb waves.



Figure 2. Electrical transmission of the delay line with (red solid curve) and without (blue dashed curve) phononic crystal.



Figure 3. Band diagram of the phononic crystal with (a) indication of respective polarizations and (b) which bands are deaf.

This result opens interesting perspectives in terms of RF components design, as they show that the frequency range where these crystals can be used as reflectors can be dramatically extended compared to only their stop band.

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Multiple Frequency Solidly Mounted BAW Filters

Research Topics : BAW Filters

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Sponsorship : STREP-MOBILIS

Partnership : Universidad Politecnica de Madrid, Aviza Technologies

Acoustic filters are an enabling technology for radiofrequency front-ends, where they are used for RF band pass filtering. CEA-Leti has focused its activities on the Bulk Acoustic Wave (BAW) filter technology, which exploits the thickness vibration of a piezoelectric thin film to synthesize RF resonators. Because of this operation frequency is to the first order defined by layer thicknesses. This means that, unlike other technologies, especially Surface Acoustic Waves (SAW) filters, the fabrication of several filters operating at different frequencies is not straightforward. Several approaches have been proposed to fabricate multiple filters on the same die, either using mass loading layers or local regrowth of piezoelectric material. In either case, this leads to a degradation of electric performances such as quality factor or electromechanically coupling factor (i.e. ultimately filter bandwidth).

To fabricate the two filters of a WCDMA duplexer on the same die, we proposed an approach based on the generation of islands with varying piezoelectric film thicknesses, obtained by deposition and selective etching of this film. This is enabled by the use of top electrodes as a selective metallic mask to the patterning of Aluminum Nitride (AIN). In the proposed design, most other layer thicknesses have been kept constant for two filters, including layers of a SiN/SiOC Bragg mirror, mass loading and passivation. Fig.1 shows a SEM cross section of the two islands, revealing the existence of two AIN thicknesses.



Figure 1. SEM cross sections of Tx (left) and Rx (right) islands.

To evaluate the impact of this multiple-frequency process on electrical performances, we measured test resonators and compared them with reference resonators with the same design, but fabricated using a conventional BAW process. As shown in Fig.2, changes in electromechanical coupling factors for the four sets of resonators required to synthesize the two filters remain within conventional fabrication dispersion, and are thus considered as neglectible.



Figure 2. Comparison of average electromechanical coupling factors between reference resonators and devices having seen the full multi-frequency process.

Fig.3 shows the response of the two filters of the duplexer measured on the same die. Insertion losses are respectively of 1 and 2.3 dB, while bandwidth exceeds 60 MHz for the two filters. Rejection will be further improved by mounting these filters onto a duplexer board with the required passives to ensure Rx-Tx isolation.



Figure 3. Transmission and reflection measurement for adjacent Rx and Tx filters.

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RF Oscillators Stabilized by Temperature Compensated LiNbO3/Quartz HBARs

Research Topics : RF Oscillators

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Sponsorship : RAPID-ORAGE

Partnership : FEMTO-ST, Senseor

The frequency stability of radio-frequency oscillators is mainly conditioned by the spectral quality of the resonator included in the oscillation loop. For midterm stability, temperature compensation is a key point. Therefore, we have fabricated temperature compensated High-overtone Bulk Acoustic Resonators (HBAR) made of a LiNbO3 thin film with (YXI)/163° orientation bonded onto an AT-cut quartz wafer. In this configuration, the thickness modes of this whole stack exhibit temperature compensation up to the third order, while revealing quality factors exceeding 25,000 in the 434 MHz ISM band [1], as shown in Fig.1. Such high quality factors are made possible by the exceptionally low acoustic losses of quartz and lithium niobate.



Figure 1. Admittance curve of an HBAR resonator operating at 434 MHz.

For proper differential operation in a Colpitts oscillator, we also investigated the use of laterally coupled HBAR resonators, whose principle is similar to monolithic quartz filters, and is shown in Fig.2: two resonators are positioned close enough for them to couple their vibrations, enabling transfer of a signal from an input to an output resonator. Provided the acoustic coupling between the two resonators is weak enough, this generates a passband narrow enough to degenerate into a simple resonance with a quality factor higher than 10,000 at 1.7 GHz [2]. This figure is already higher than the one obtained with state of the art double mode SAW resonators.



Figure 2. Evanescent coupling between vibrations of two high-overtone bulk acoustic resonators.

Filters and resonators have been introduced in a Colpitts-type negative resistance circuit whose phase noise has been measured. Fig.3 shows the phase noise of two oscillators based on laterally-coupled HBARs operating respectively at 935 and 1636 MHz, compared to the phase noise of a reference oscillator stabilized by a conventional quartz resonator operating at 100 MHz. Although the later seems to exhibit much better phase noise performances, this low frequency source would require to be multiplied by a factor 16 to reach 1.6 GHz, resulting in an additional +12 dB phase noise which would lead in practice to a -140 dB noise level at 10 kHz offset from the carrier frequency. Therefore, this solution would not provide better performances than our filters.



Figure 3. Phase noise measurements of HBAR oscillators.

Future work focuses on optimizing the filter and oscillator structure to improve quality factors in order to decrease further phase noise.

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Film Bulk Acoustic Resonators based on Single Crystal Piezoelectric Thin Films

Research Topics : Single Crystal Thin Films, BAW Resonators

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Sponsorship : ANR-POEM, RAPID-ORAGE

Partnership : RHEA, FEMTO-ST, SOITEC

Performances of acoustic devices are driven by the material properties of the piezoelectric films employed in their fabrication. Conventional Bulk Acoustic Wave (BAW) resonators operating at GHz frequencies are based on Aluminum Nitride (AIN), which exhibits piezoelectric properties sufficient for historical applications, but which starts revealing limited for emerging applications. In this context, CEA-Leti investigates alternative materials or other deposition processes.

A first challenge acoustic resonators have to face is the increase in operating frequency of new standards. Conventional devices target frequencies from 1.5 to 2.5 GHz, where AIN layers in the 500 nm - 2 µm range are appropriate. To reach higher frequencies, thinner films are needed, but it is well known that in this case sputtered films suffer from poorer piezoelectric properties. To overcome this degradation, we elected to deposit 50 nm of AIN by Molecular Beam Epitaxy onto a silicon substrate. Subsequent processing involved deposition and patterning of a top electrode, deep reactive ion etching of silicon on the backside and deposition of metal on the bottom of the exposed film, so as to form a Film Bulk Acoustic Resonator (FBAR) operating at 16 GHz [1], whose response is shown in Fig.1. At the present time, this is the highest frequency FBAR device reported so far.



Figure 1. Measurement of a 16 GHz FBAR based on an epitaxial AIN thin film.

Another challenge is the increase in filter bandwidth, related to the need for higher data rates in wireless applications. For this, piezoelectric materials with better properties than AIN are required. Several years ago, CEA-Leti has started to investigate the transfer of thin layers of LiNbO3 onto host substrates using the Smart CutTM technique. We recently introduced a new approach to form free standing piezoelectric membranes in order to build FBARs. Fig.2. shows the electrical response of a first prototype operating at 2.4 GHz [2]. A strong spurious response is still visible at 3.4 GHz and is attributed to resonances of parts of the resonator out of the membrane, but it will disappear in future iterations with an improved fabrication process.



Figure 2. Measurement of a 2.4 GHz FBAR based on X-cut LiNbO3 thin film transferred by Smart CutTM.

Finally, a third challenge is the fabrication of high frequency quartz resonators integrated onto silicon. Such resonators could be efficiently used as a replacement to the bulky conventional quartz resonators in time references, which can currently not be integrated easily. As a first step towards this goal, we investigated the transfer of thin quartz layers onto silicon, using direct bonding of quartz on silicon and then grinding of the quartz wafer down to 10 μ m. By a process similar to the one performed with epitaxial AIN, we successfully fabricated a quartz FBAR operating at 190 MHz whose response is shown in Fig.3 [3].





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Millimeter-Wave Interconnects for Advanced 3D Silicon Interposers

Research Topics : RF interconnects, Silicon interposers, TSV

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Silicon 3D integration is considered as one of the most promising solutions to overcome 2D scaling limitations and to enhance the performances of electronic products. Silicon interposers, or "2.5D integration", opportunity to realize offer the multi-chips interconnections and heterogeneous technology stacking while integrating specific passive devices like decoupling capacitors, high-Q inductors or antennas on the silicon carrier. However 2.5D or 3D integration technologies comprise several basic interconnect elements, such as Through Silicon Via, Redistribution Layers, Cu-Pillar and bumps to transmit signals inside circuits (Fig.1). The impact of the interconnect elements on high speed signal integrity all along the global 3D interconnection chain requires investigation and all interconnects have to be accurately modeled to give some major rules to follow in terms of routing, chip stack orientation and technological options to design 3D products [1].

As a large range of silicon oxides is available to realize interconnects, choice has to be made depending on dielectric losses and low permittivity but also front side, back side and TSV processes compatibility. A wide variety of oxide insulators have been evaluated up to 60 GHz and losses mechanisms, including in particular charge effect at the interface between silicon and silicon oxide, have been highlighted [2]. It appears that thermal oxide is the best choice to passivate the silicon substrate and that performances good RF for millimeter-wave interconnects can be achieved on insulator compatible with front-side routing technology of the interposer by using PECVD oxides deposited at temperature below 400°C. PECVD oxides offering good compromise between RF performances and low temperature (below 250°C) compliant with TSV passivation and back side RDL have also been found (Fig.2).

Together with this first study, a silicon interposer with TSV interconnects has been fabricated and characterized up to 50GHz. Measurements and 3D-EM simulation demonstrate major influence of charge effects created at the High resistivity silicon substrate and back-side low-temperature SiO2 material interface. Technological and design optimizations to reduce impedance mismatch and substrate influence have been detailed to achieve significant insertion loss reduction [3]. Measured loss per TSV of 0.5dB at 50GHz should be decrease down to 0.3dB (Fig.3) by increasing pitch of the transition and by using optimal low temperature PECVD SiO2 material to reduce substrate parasitic conductivity.

Partnership : ST Microelectronics, IMEP-LAHC



Figure 1. Face to face stacking on silicon interposer.



Figure 2. Attenuation constant at 5GHz, 20GHz and 60GHz for wafers with various oxide insulators.



Figure 3. Insertion loss of back-to-back transition in 0.1-50GHz bandwidth.

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MEMS Actuators & Sensors & Reliability

- Macro Energy Harvester based on Aluminium Nitride Thin Films
- Shape Memory Alloy/Piezoelectric Composites
- Electrocaloric Effect on Ceramics and Polymers
- Single Crystals Piezoelectric Thin Films on Silicon
- PZT Membrane Actuator Design
- Wavelens: Thin Varifocal Liquid Lenses Actuated Below 10V for Mobile Phone Cameras
- Surface Acoustic Wave Vacuum Sensor
- Suspended Piezoresistive Silicon Nanowires for NEMS
- A New Compact 3D Accelerometer with High Sensitivity using Nanogauge Piezoresistive Detection
- Mass Spectrometry with a Nanomechanical Resonator for Mass Measurement of Neutral and Ionized Biomolecules
- Nano-Indentation Contact Study for Micro-Switch Applications
- Dielectric Charging in RF MEMS Electrostatic Switches

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Macro Energy Harvester based on Aluminium Nitride Thin Films

Research Topics : Piezoelectric, Energy Harvesting

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Sponsorship : MINALOGIC-SAMEE

Partnership : Schneider, Alpwise, E2V, Maya-Technology,IS2T

With proliferation ultra-low the of power consumption wireless devices and the green concern, a current trend is to take advantage of energy harvesting. This can performed from mechanical vibration, electromagnetism, temperature and so on. Most of the vibration energy is between 50 and 200Hz and the related acceleration is often no more than 1-2 m.s-2[1]. Besides, for low power communication devices, 10 to 100 µW is considered to be the minimum energy target range to be collected continuously. Therefore, to reach this energy target with such a low acceleration and frequency, the needed device surface lies in the cm² range. Our study consists to the fabrication and characterization of cantilevers with Aluminium Nitride (AIN) piezoelectric thin films, adapted to such a kind of weakly vibrating environment (100 Hz - 1m.s-2).

To obtain a maximum charge displacement under mechanical vibration, AIN films of 5.6μ m thick were deposited by dc-pulsed reactive sputtering. One of the key processes is to perform large electrodes (typ. 1 x 2 cm²) to extract the maximum charges from the cantilever vibration. A back side etching is performed to decrease the resonance frequency of this 2.6cmlong cantilever to obtain a resonant frequency of the environment (cf. Fig.1).



Figure 1. sketch of cantilevers cross sections developed in this study.

Moreover, a metallic mass can be added at the free end of the beam to reduce and adjust this resonance frequency. A vibrating device is used to generate a controlled acceleration to the cantilever. The charges generated by the piezoelectric film are collected directly on an oscilloscope to be analyzed.

Once the device was validated by this measure, we studied the effect of the impedance by placing a resistor between the cantilever and the oscilloscope. As a result we find that optimal impedance permits to increase by 25% the maximum power harvested (Fig.2).

Moreover we developed an electrical circuit of management by the use of a diode bridge to rectify the signal and a capacitor to obtain a continuous voltage suitable to aliment device (Fig.3).



Figure 2. Power versus impedance, with R=1M Ω (oscilloscope) P=86 μ W, optimum for R=470k Ω , P=117 μ W, rise of 25%.





As a proof of concept, a test vehicle consisting of a LED which flash once sufficient power is harvested, has been designed (Fig.4).



Figure 4. Photo of the harvester and the test vehicle.

The interest here is that each flash of the Led corresponds in energy of sending about 12 octets with a wireless emitter. At 0.1g, the Led flash with a period of about 10s and at 0.3g this period become 500ms which is very suitable to developed autonomous communicant sensor. Finally, studies on packaging have to be made in order to increase harvested power.

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Shape Memory Alloy/Piezoelectric Composites

Research Topics : MEMS Actuators, Energy Harvesting

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Sponsorship : CARNOT-MANDARIN, RTRA

Partnership : G2ELab, MEPhI Moscow

The increasing demand in alternative energy sources for low-power electronics and autonomous wireless sensors has given rise to substantial research activities in the field of energy harvesting. Among the different energy sources, thermal sources are widely available. Thermal energy can be directly converted into electricity by means of thermoelectric (Seebeck effect) or pyroelectric materials. Another scheme is to indirectly convert heat into electricity through mechanical transformations.

LETI and G2Elab have reported new thermal energy composite harvesters based on the coupling of shape memory alloy (SMA) and piezoelectric materials (PE) [1-2]. The composites are realized by assembling NiTi(Cu) shape memory alloys with PZT. The SMA material stretches or shrinks with temperature variations; the resulting mechanical stress is converted into electrical energy by the piezoelectric layers. SMAs combine large motion and relatively high forces in a small active volume, thus providing high output. Fig.1 and Fig.2 illustrate two types of connectivity for the SMA/PE composites. The main benefit of the SMA/PE composites over standard thermoelectric energy harvesting systems is the ability to harvest very small ambient thermal variations (without cold source), from \pm 1°C to \pm 10°C depending on the composition of the SMA. It also works on a quasi-static mode which means it can harvest energy from random thermal fluctuations. Therefore SMA/PE composites are broad band (DC to kHz) and provide high voltage (up to 200 V) compared to state of the art piezoelectric harvesters, which are resonant systems and thus need to be mechanically tuned to the exact frequency of the targeted vibration.

The preliminary SMA/PE composites were able to harvest energy up to 300 uJ per temperature transition (see Fig.3) which was generated for a reduced volume of active material of about 0.1 to 0.2 cm3. This energy level may be enough to power a standard wireless sensor. It is estimated that optimized systems (better mechanical coupling, better heat transfer) could produce up to 1 mJ/mm3 of useful electrical energy.



Figure 1. "Iaminated" SMA/PE composite with TiNiCu ribbon glued onto commercial PZT-MFC (microfiber composite) with cyanoacrylate glue.



Figure 2. "Juxtaposed" SMA/PE composite with NiTi wire bent on a plexyglass system and connected to a PZT double-slab.



Figure 3. Output voltage generated by SMA/PE composites from heating and cooling across the thermoelastic transition temperature region.

LETI is now moving to the next step with the silicon integration of shape memory alloys. SMA/PE thin film composites will lead to higher mechanical coupling between layers and more efficient thermal management. Moreover, the resulting miniaturization will provide new possibilities of application such as thermal energy harvesting directly close to calculator chips into a computer or microcontroller chips in a smart card. The SMA/PE composites will offer renewable sources of energy and freedom from traditional batteries for many markets.

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Electrocaloric Effect on Ceramics and Polymers

Research Topics : Materials, Electrocaloric Effect

E. DEFAY, (N. MATHUR)

Sponsorship : CARNOT Funding

Partnership : Cambridge University

An applied electric field can reversibly change the temperature of an electrocaloric (EC) material under adiabatic conditions, and the effect is stronger near phase transitions. Dr Mathur and his team from University demonstrated Cambridge а giant electrocaloric effect ($\Delta T=12^{\circ}K$) in 350 nm thick perovskite PbZr_{0.95}Ti_{0.05}O₃ (PZT) polycrystalline films near the ferroelectric Curie temperature of 222°C [Science, 311, 1270 (2006)]. Apart from perovskite thin films, polymers and more specifically PVDF films exhibit a strong EC effect closer to room temperature (ΔT=12°K at 60°C) [Science, 321, 821 (2008)]. This large electrocaloric effect in thin films can potentially find application in electrical refrigeration and more specifically in cooling for integrated circuits. Here we aim at comparing polymers and PZT-like materials in order to get a clearer picture from the application point of view.

The EC effect can be characterized by measuring the variation of temperature (ΔT) experienced by the EC element once a strong voltage is applied as sketched in Fig.1. This weak reversible variation of temperature (0.35°K) is experienced by a 1mm³ stand-alone Multi Layer Capacitor (MLC). In this case, the active EC material is BaTiO₃. This is so far the only EC object where ΔT can be measured directly, thanks to the rather big volume exhibited by the MLC. Let us remind that the EC effect is induced by a strong variation of the entropy variation is a consequence of the strong variation of polarization taking place in EC materials.



Time (s)

Figure 1. Variation of temperature experienced by a MLC after applying 200V at t=3s and removing it at t=18s. The effect is reversible.

In the framework of our current project with Cambridge Univ. on EC materials, LETI set up an infrared (IR) camera able to observe the small ΔT of this MLC as observed in Fig.2.



Figure 2. ΔT experienced by a MLC as observed by an IR camera. a, b and c correspond to the point reported in Fig.1.

For thin films, measuring the direct ΔT is still an issue as the variation of heat is rather small, though the variation of T° can reach more than 20K. Therefore, it is usually assessed via the so-called indirect method which is based on thermodynamic calculations and consequently on the following equation:

$$\Delta T = -\frac{1}{\rho C} \int_{E_{\min}}^{E_{\max}} T \left(\frac{\partial P}{\partial T} \right)_{E} dE \tag{1}$$

This method has been applied to PZT and PVDF and the main results are gathered in the following Table [1].

Table 1. Main EC parameters extracted from PZT and PVDF thin films.

Material		PZT	PVDF
Entropy	kJ K ⁻¹ m ⁻³	62	97
Heat	J cm ⁻³	31	35
Temperature	K	12	12
Electric field	kV cm ⁻¹	480	2000
Dielectric constant		750	70
T _c	°C	222	80

Therefore, it is remarkable to observe that PZT and PVDF thin films exhibit basically the same entropy, heat and T° variation for a given volume whereas they exhibit completely different dielectric properties, as proved by their dielectric constant and the maximum field they can withstand.

The next step of our study is to predict and measure the coefficient of performance of these films in the case of an ideal refrigeration cycle.

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Single Crystals Piezoelectric Thin Films on Silicon

Research Topics : Materials, Piezoelectric Devices, Actuators

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Sponsorship : ANR-MOCA

Partnership : INL Lyon

Thanks to roughly two decades of research and development, the integration of polycrystalline PZT thin films on Si is currently possible. However, one can guess that single crystal PZT could improve the behavior of PZT thin films. Several previous works on single crystalline PZT films have already shown its excellent electrical properties, namely large piezoelectric coefficients (d₃₃). But the remaining problem to integrate them on Si in the epitaxial context is the lattice mismatch and the chemical stability with Si. Strontium Titanate (SrTiO₃) has been regarded as the ideal template to deposit most of functional oxides, due to the low lattice mismatch with Si (1.68%) and chemical compatibility. For example, it is well known that Pb(Zr,Ti)O₃ (PZT) can easily react with Si and the interdiffusion of Pb and Si at the PZT/Si interface occurs even at a temperature as low as 500 °C. The possibility to grow epitaxial SrTiO₃ (STO) on Si substrate paves the way for the integration of complex perovkiste-type oxide onto silicon substrate.

In this study, we have successfully deposited 70nmthick single crystalline $Pb(Zr_{0.52}Ti_{0.48})O_3$ thin films on SrTiO₃-buffered Si(001) substrate by the sol-gel method. Note that MBE was performed at INL. This original approach is interesting as it gives the opportunity to shorten the time to applications, as sol gel is now considered as a rather industrial way of performing PZT. The chemical composition of PZT is Zr:Ti=52:48 as this last exhibits the largest piezoelectric coefficients near the so-called morphotropic phase boundary (MPB). The single crystalline structure was checked by x-ray diffraction (XRD) as observed in Fig.1.



Figure 1. Pole figures of PZT/SrTiO3/Si(001) on different reflections: left) PZT(002); right) PZT(202).

In these pole figures, the fourfold symmetrical PZT(202) reflections around the central PZT(002) reflection demonstrate the single crystalline nature of this PZT epitaxial film on SrTiO3 template in cube-on-cube mode.

References

Therefore, ferroelectric domains were created by applying a voltage using a Piezoelectric Force Microscopy (PFM) setup. An artificial ferroelectric domain was created and visualized in this PZT film as shown in Fig.2. $10 \times 10 \mu m^2$ surface was scanned and poled by +6V dc voltage applied on the cantilever tip, then followed by -6V dc voltage to reverse the piezoelectric dipoles in a smaller area ($5 \times 5 \mu m^2$) at the center. A 1V-amplitude and 4kHz-frequency ac signal was then applied to collect the out-of-plane piezoelectric response. Both the amplitude and the phase of the PFM signal were recorded simultaneously with the topography. In the "up" domain, the poling is uniformly and completely achieved inducing intense amplitude and a saturated phase shift.



Figure 2. Artificial domains created by PFM in epitaxial PZT thin film: the amplitude (left) and the phase (right) of PFM signal.

Besides, C-V curves exhibit a typical ferroelectric hysteresis loop with a rather low dielectric constant (ϵ_r =100) because of the lack of a proper bottom electrode. Moreover, these films exhibit low leakage currents, namely 100nA/cm² at 600kV/cm [1].

These results are evidences of a very promising technology as this film is the very first one of this kind ever performed and characterized at LETI. New results are to come in the next few months as all the partners in the MOCA project have been provided with new films. The foreseen applications are mainly actuators and resonators.



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Research Topics : Materials, Piezoelectric Devices, Actuators

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Partnership : STMicroelectronics, IEMN-ISEN

Piezoelectric actuation is under interest because it allows obtaining integrated and performing devices which can be used in many fields of applications (loudspeaker, inkjet, drugs delivery, sensors...). In particular, we proposed to study Pb(Zr0.52, Ti0.48)O3 (PZT) actuators due to the high PZT piezoelectric coefficient. We present the Finite Element Method (FEM) study of the optimum PZT-actuated membrane electrode design.

We used the FEM CoventorTM software to study PZTactuated membranes. Firstly, we study the membrane shape influence. We know that the membrane displacement (for a given actuation voltage) depends of the membrane sizes: the larger the membrane, the larger the displacement as shown in Fig.1 (W1>W2>W3>W4). Then we can observe that there is a weak influence of the rectangular membrane width over length ratio. The smaller membrane size (width) will govern the membrane behavior. It is worth noting that a circular membrane (radius R) and a rectangular membrane (width=2R) present the same order of magnitude of maximum displacement (Table 1, $\Delta \approx 6\%$). Thus, for compactness purposes, we can privilege a circular membrane shape.

Secondly, for a given membrane surface, we study the piezoelectric actuator surface influence. Fig.2 shows the rectangular membrane normalized differential displacement (membrane displacement under a given actuation voltage minus membrane displacement under OV, normalized with regard to the maximal value) over the membrane surface on the piezoelectric actuator surface ratio variation. The same study was performed on a circular membrane (Fig.3). This study shows that for both rectangular and circular membrane, the same order of magnitude of membrane surface on actuator surface ratio (50-60%) allows obtaining the higher membrane differential displacement. We will retain this design rule for our future piezoelectric actuator design.

Table 1. Rectangular and circular membrane normalized differential displacement comparison.

Design	Rectangular	Circular
Sizes	2R×2R	Diameter: 2R
3D view		
Normalized differential displacement (same voltage)	-100%	-93.7%



Figure 1. Rectangular membrane normalized differential displacement versus membrane width over length ratio.



Figure 2. Rectangular membrane differential normalized displacement versus the membrane surface on the piezoelectric actuator surface ratio.



Figure 3. Circular membrane differential normalized displacement versus the membrane surface on the piezoelectric actuator surface ratio.

For predictive simulation, material properties must be accurately defined. Picosecond ultrasonic characterization can be used to define exactly the mechanical properties of the simulated materials. The piezoelectric coefficient (d31) should be equally characterized. Finally, the FEM models should be compared to demonstrator measurements.

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Wavelens : Thin Varifocal Liquid Lenses Actuated Below 10V for Mobile Phone Cameras

Research Topics : MEMS Actuators, Optical

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Sponsorship : OSEO-MINIMAGE

The camera modules in mobile phones are currently using voice coil motors (VCM) to tune the focal length of the optical system and to perform auto-focusing. However, the specific constraints related to the integration into mobile phones, i.e. drastic size control, low power consumption and above all cost, make VCM less and less competitive as new products emerge. In order to overcome these issues, variable-focus (or varifocal) liquid lenses were proposed to provide more compact imaging optical elements. The Wavelens technology we have developed is made of a deformable membrane varifocal lens with embedded micro-electromechanical system actuator (Fig. 1).



Figure 1. Operating principle of the Wavelens varifocal lens.

The lens is made of a polymer membrane that encapsulates a high permittivity liquid in a cavity on top of a glass wafer. Annular electrodes situated below the membrane and on the glass wafer form the electrostatic MEMS actuator. By applying a voltage between the electrodes, the electrostatic actuation generated reduces the gap and pushes the liquid towards the center of the lens changing the curvature of the membrane (see Fig.1).

The patented fabrication process flow [1] is the following: on a 200mm silicon wafer, a polymer membrane and a first annular metal electrode are defined by conventional deposition, lithography and etch steps. On a 200mm glass wafer, the second annular metal electrode is created similarly, followed by the definition of a circular cavity using photosensitive materials. A high permittivity liquid is then dispensed in the cavity. Finally, the two wafers are assembled by polymer bonding, the Si wafer is thinned down and the membrane is released by conventional deep reactive ion etching. The 3mm optical area is defined by the electrodes inner diameter for a total lens outline of less than 6 6 0.65mm. Close-up pictures of a liquid lens are shown in Fig.2. Since most of the technological steps come from microelectronics processes, the lenses can be manufactured with an excellent accuracy at a very low cost.



Figure 2. Close-up pictures of a varifocal lens.

As underlined by multi-physics FEM simulations a specific attention must be given to the mechanical properties of the membrane and electrode materials in order to optimize the actuation.

Two membrane materials where investigated: a xylylene-based polymer (membrane A) and a siloxanebased polymer (membrane B) [2]. By using membrane B, the residual stress is kept almost independent of the post-process temperature (see Fig.3). Combined with a reduced Young modulus this improves the overall rigidity of the membrane.



Figure 3. Membrane residual stress evolution with the postprocess temperature.

At the electrode level an optimization of the materials mechanical properties, in particular a low equivalent residual stress, is also needed. Very low actuation voltages are targeted when optimizing the mechanical properties of the membrane and of the electrodes: a refractive power variation of 15m⁻¹, that is required to perform auto-focus, is forecasted below 10V applied voltage. This low actuation voltage can permit to avoid the development of a costly, specific driver and simplifies the integration of an auto-focus system with the Wavelens technology.

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Surface Acoustic Wave Vacuum Sensor

Research Topics : MEMS

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Sponsorship : ANR-PASCAL

Partnership : ADIXEN, UJL, SENSEOR

There is growing demand for very small vacuum sensors as the size reduction paved the way for new applications of integrated sensors. Most of the applications deal with the integration into pumping structures and stages to monitor pumping device performances and vacuum level. Also, cheap sensors capable to measure vacuum over the whole 10⁻³ to 10⁵ Pa range are not available and usually two vacuum sensors are combined in one single gauge to cover wide pressure ranges. The only competitors in this pressure range are micro-Pirani gauges, but these gauges are complicated to fabricate because they require micro machining techniques, which also remain expensive.



Figure 1. Pictures of the SAW vacuum sensor.

Another way to achieve large pressure range is to use a SAW (Surface Acoustic Wave) sensor, whose frequency varies with the gas thermal conductivity, just as Pirani sensors. SAW sensors are interesting because they can be easily designed at frequencies compatible with current electronic components. Also, they have a large sensitivity and a low fabrication cost as it is a well spread technology.



Figure 2. Test bench for the SAW vacuum sensor.

The sensor operating principle is based on the gas thermal conductivity variations with the vacuum level. The SAW device is heated at a temperature much higher than the gas temperature by Joule effect. At a given constant pressure, a thermal equilibrium takes place and the SAW frequency stabilizes. When the pressure decreases, the number of gas molecules decreases, which changes the thermal conductivity of the gas. Then the SAW sensor temperature rises as it is less cooled down and its frequency shifts.

The SAW sensors are fabricated on a black lithium niobate substrate using conventional microelectronic fabrication process. Then, they are diced and soldered on a polyimide film before being mounted on a Printed Circuit Board (PCB) as shown in Fig.1.

A test bench has been developed to characterize the sensor; it is presented in Fig.2. The sensor is placed in a chamber where the pressure can be changed by a manual variable leak valve. A SourceMeter is used to control the heating current in the resistor (Joule effect) and the RF signal of the SAW is measured by a vector network analyzer. Also, a calibrated pressure gauge is used as a reference and the temperature in the chamber is monitored.



Figure 3. Measurement range and response time.

The measurement results presented in Fig.3 illustrate the current variation as a function of the pressure. The discontinuity in the data is due to the fact that two different gauges are needed to cover the whole pressure range. The results demonstrate that the sensor is sensitive to pressure variations in the 10-3-105 Pa range with a very good sensitivity. Also, the response time, which is the delay required by the current to stabilize at a constant value after a pressure variation, has been measured. It is 5s as presented in Fig.3.

A new generation of acoustic devices is already under development, the goal of these new devices is to demonstrate that the response time can be improved to compete with the fastest vacuum sensors on the market. Also a new implementation on a PCB is currently studied to improve not only the response time but also the sensitivity of the SAW-Pirani vacuum sensor.

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Suspended Piezoresistive Silicon Nanowires for NEMS

Research Topics : NEMS

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Sponsorship : CARNOT-NEMS, FP7-NEMSIC

Partnership : University of Lyon I-CNRS, CALTECH

MEMS miniaturization paves the way towards smaller systems in the range of a few nanometers called NEMS (Nano Electro Mechanical Systems). Following this trend, silicon nanowire resonators have been fabricated with top-down techniques used currently in microelectronics industry. Up to date, it is the only example of top-down silicon nanowire NEMS. Thanks to their compatibility with microelectronic tools, nanowire resonators and CMOS circuits can be integrated on the same substrate resulting in complete system integration: device + electronics on the same chip. This approach can improve the device response and enable the use of ultra-scaled detectors.

Silicon nanowire resonators fabricated at LETI have integrated electrostatic actuation and selftransduction based on the piezoresistive effect of second order. When entering in resonance, a resistance variation occurs due to mechanical internal strains; this resistance variation is used to transduce the resonance response. The width of these nanowires varies between 50 and 320 nm, while their thickness is set to 160 nm. An example of suspended silicon nanowire devices is shown in Fig.1.



Figure 1. Silicon nanowire resonator 80nm wide and 160nm thick.

The piezoresistive coefficients of the silicon nanowires were extracted by strain - resistance measurements with the four-point bending method [1]. The extracted gauge factors are in the range of the bulk silicon (varying from 68 to 235 for suspended nanowires). In Fig.2, measurements for three identical devices show low dispersion and demonstrate the repeatability of the fabrication process chosen.

Next step is the realization of dynamic measurements (Fig.3) to confirm the functionality of such devices. Knowing the gauge factor and considering small displacements in dynamic regime (lower than 1 nm), an estimation of the detection current can be given by applying the equation:

$$I_{nems} = \frac{V_{ds}}{R} \times \frac{G\pi^2}{4} \left(\frac{x}{L}\right)^2$$

where Vds is the nanowire polarization, R its resistance, G the gauge factor, x the displacement and L its length.



Figure 2. Resistance variation with strain for silicon nanowires 1 μm long, 36 nm wide and 38 nm thick.



Figure 3. Example of a resonance measurement for a silicon nanowire with dimensions L=2.5 μ m, w=80nm and t=160.

Potential applications for resonant NEMS are mass or gas sensing and time reference applications. In fact, when molecules are absorbed on the nanowire surface, the total mass of the nanowire increases; this increase leads to a shift of the resonance towards smaller frequencies. The relative frequency shift per unit of mass accounts for the sensitivity of the detector. With such small devices it has been shown that molecules with a mass down to some zg (10^{-21} g) can be detected.

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A New Compact 3D Accelerometer with High Sensitivity using Nanogauge Piezoresistive Detection

Research Topics : Inertial MEMS, Silicon Nanowires, Piezoresistivity Transduction

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Sponsorship : Nano-Innov

Partnership : IM2NP

This paper outlines a 3D accelerometers based on piezoresistive nanogauges. The devices combine MEMS and NEMS technologies to benefit from high inertial force sensitivity of MEMS mass and high force sensitivity of nanogauges due to their small cross section ($250 \times 250 \text{ nm2}$, $5\mu \text{m} \log$). It allows for a given acceleration range a drastic reduction of the inertial mass size, thus increasing the MEMS sensors integration ability: for instance, 10g full scale accelerometers are designed with mass area as low as 0.1 mm2 ($300 \times 300 \mu m2$). 3D accelerometers area is smaller than 1 mm2 including packaging.



Figure 1. Principle of in plane M&NEMS. A large inertial mass (1) is connected to the substrate by two suspension beams (2), set perpendicular to each other, and two piezoresistive nanogauges (3) are located on each side of the mass arm. The two suspension beams allow rotation motion around their intersection axis. When undergoing an inertial force, the whole mechanical system turns around its pivot, thus applying opposite magnified forces on each nanogauge.

In the state of the art, first silicon piezoresistors were diffused at the surface of beams undergoing mechanical stresses. Then suspended silicon gauges were implemented to sense inertial force applied on the mass. However gauges size remained in the micrometer range ($2 \times 50 \times 100 \mu m3$), thus generating a low force sensitivity and only in-plane motion could be sensed. Here, these two limitations can be addressed by the M&NEMS concept, in which suspended silicon nanogauges are etched in a NEMS layer (250 nm) and inertial mass in a thicker MEMS layer ($10 \mu m$) (Fig.1 and Fig.2). Fabrication process [1,2,3] requires only six mask levels. The high in-plane sensitivity results from the force magnification caused by lever arm effect and

the concentration of this force on a very small area (250x250nm²) generating large stress in the nanogauges. The out-of-plane detection takes advantage of the two thicknesses to transfer the inertial force into the MEMS plane.



Figure 2. SEM photograph of the 2 silicon nanogauges of a XY accelerometer.

Electromechanical characterizations show excellent agreement with device models. Nanogauges from a same bridge exhibit a discrepancy of 1%, due to the weak local dispersion on etching features. Sensor offset dispersion should be around 33% of full scale. Temperature coefficient of resistance is evaluated at 1360ppm/°C with 30ppm/°C dispersion. Basic thermal compensated measurement scheme, like Wheatstone bridge, therefore exhibits temperature offset sensitivity around +/-0.15%/°C of full scale. Mechanical responses were tested with gravity force. Fig.3 displays the accelerometer signal as a function of the tilt angle. Yield as high as 97% have been obtained for the most robust designs, thus showing a good maturity of the manufacturing technology.



Figure 3. Accelerometer response to gravitational force as a function of tilt angle. The device is placed on a vertical rotation plate.

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Mass Spectrometry with a Nanomechanical Resonator for Mass Measurement of Neutral and Ionized Biomolecules

Research Topics : NEMS, NEMS VLSI, Mass Spectrometry

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Sponsorship : CARNOT-NEMS

Partnership : CALTECH

The topic of this study is a novel mass spectrometry method that uses a nano-electromechanical system (NEMS) as the mass detection element for a matrix assisted laser desorption ionization-mass spectrometry (MALDI-MS) system [1]. A NEMS device is an on-chip nano-fabricated mechanical resonator whose frequency can be tracked electronically. Such devices come in a broad range of geometries and have been used for a variety of sensing applications including mass detection [2]. The theoretical mass resolution of these devices is estimated to be 1Da, demonstrated experimental mass resolution below 100Da.



Figure 1. The NEMS device used [2].

The principle is the following: the mechanical resonator is electronically driven at its resonance frequency, f0. When a biomolecule lands on the resonator, it changes the resonator mass, M, by a small amount δm . In the limit of $\delta m << M$, the mass change linearly shifts the resonator frequency by some amount, Δf . By tracking the resonant frequency of the NEMS in real time using a phase locked loop, one can measure the temporal frequency shift, Δf , and thereby calculate the mass of an individual biomolecule.

We have combined the above-described NEMS cantilever mass detector with a MALDI-MS system. A representative doped Si device is shown in Fig.1. The doped Si cantilever is clamped at one end and free at the other (top picture, Fig.1). A gate electrode is used to actuate the cantilever using electrostatic actuation (blue area, bottom picture, Fig.1). Two piezo gauges near the clamped end (red and green) are biased with opposite polarity to produce a signal proportional to the motion of the resonator which is then read out at the base of the cantilever.

A schematic of the MS system is shown in Fig.2. A NEMS device is fabricated on a silicon chip that is mounted on the end of a cryostat inside of an ultrahigh vacuum chamber. A stainless steel MALDI sample plate is mounted nearly parallel to and 1cm away from the device chip. A N2 laser (337nm) strikes the MALDI sample plate and the ejected particles adsorb onto the NEMS surface, which has been cryogenically cooled to 77 Kelvin.

The proposed system has several important advantages over traditional MALDI-TOF systems.

First, our system can detect particles as large as ~30GDa, giving it a much larger dynamic mass range than any current MS system and can maintain the same mass resolution (50kDa) for all mass ranges.

Second, the NEMS detector is sensitive to both ionized and neutral species. The ionization efficiency of MALDI may be as low as 1 part in a thousand. Our system could potentially realize a 103 increase in sensitivity over current MALDI-TOF instruments. This is critical for applications involving small biological samples and especially for recording protein/peptide spatial distributions as in imaging mass spectrometry (IMS) of small tissue sections.

Finally, our system offers the potential to achieve efficient sub-cellular MALDI-IMS, a goal that continues to evade present researchers. In addition to the enhanced sensitivity and dynamic mass range, our detectors can be placed very close to the sample surface, allowing for significantly increased spatial resolution of protein images in tissue sections or even single cells.



Figure 2. Schematic of the MS System.

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Nano-Indentation Contact Study for Micro-Switch Applications

Research Topics : Nano-Indentation, Rough Contact, Micro-Switch

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Sponsorship : ANR-FAME

Partnership : Microelectronics Center of Provence, EMSE

MEMS ohmic switches have demonstrated interesting performances due to their low electrical contact resistance which depends on multiple contributions. One important of them is the roughness of the contact area. The contact area is indeed composed by clusters of asperities that have different sizes, heights and curvature radii.

This work [1] investigates the discrete mechanical deformation of gold thin film asperities at the nanoscale within micro-switches pressure range (100MPa-1GPa) in the case of a sphere/plane contact configuration. For this purpose, loads from 250µN up to 2mN are applied by a nano-indenter with a spherical diamond tip (50µm curvature radius).

Before and after indentation loading, the contact area is investigated by SPM topography measurements and treated by specific digital image processing [2]. During this procedure nearly 80% of the surface asperities are matched one to one before and after indentation. For each applied load, the asperities in plastic deformation mode are then identified, sorted and used to determine a value of "surface hardness".



Figure 1. Comparison between calculated and experimental asperity height after a 2mN load. XR is the radial position relative to indent center.

This hardness is first evaluated by comparison of plastically deformed asperities residual height with Bahrami's sphere / plan rough contact model (Fig. 1).

Then, the real area of contact is evaluated summing the contact area of each deformed asperity determined by the Abott and Firestone truncation model. This allows a second evaluation of Asperities hardness.

Results are similar (Fig.2) with the two models and show that asperities or "surface" Hardness decreases from 2GPa at low load down to the 1GPa intrinsic gold thin film value at high load.



Figure 2. Hardness determined following Bahrami and Abbot & Firestone models.

This result is coherent with the hardness measured by classical Berkovich nano-indentation using the continuous stiffness measurement technique [3] showing also a decrease from 2GPa at a 10nm depth down to 1GPa at 200nm. This indent size effect (ISE) can be attributed both to surface effects and plasticity size effects. This study clearly shows that ISE has to be taken into account in the understanding of contact tribology for micro-witches.

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Dielectric Charging in RF MEMS Electrostatic Switches

Research Topics : RF MEMS Switches, Reliability

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Sponsorship : ANR-FAME, ESA, CNES

Dielectric charging is the key failure mechanism of the electrostatically actuated RF MEMS switches. It consists in trapping parasitic charges and leads to a dramatic drift of the pull-in voltage. This failure mechanism has not been fully understood yet because, in particular, the dielectrics used are deposited by PECVD process and we lack fundamental knowledge on such materials. That's why CEA-LETI has directly investigated, for the first time for MEMS, the trapping properties of bulk PECVD dielectrics to build an original time predictive model applicable for electrostatic MEMS switches. As a reminder, the common ways reported in the literature to study the dielectric charging of RF-MEMS switches are based on switching tests, analysis of I-V sweeps, TSD currents, charging and discharging currents, Kelvin force microscopy.

Our CEA-LETI time predictive model simulates the drift of the pull-in voltage due to dielectric charging. The originality of this model lies in the introduction of a trapping rate variation which simulates the time effect [1]. The trapping rate depends on 3 main factors: the amount of injected charges, the capture cross section which determines how efficiently these injected charges are trapped and the number of available empty traps. These 3 factors define the trapping properties and are extracted from the mechanisms of conduction and the mechanisms of trapping respectively characterized by I-V sweeps and constant current injections performed on Metal-Insulator-Metal capacitor.

SiNx and SiO2 PECVD dielectric materials are currently used for CEA-LETI RF-MEMS switches and their trapping properties have been investigated to quantify the charge accumulation by means of our model. The simulated results are fully consistent with experimental data obtained for electrostatic MEMS switches made with these materials (see Fig.1). Consequently, the model can be successfully used to compare various dielectric materials, and to lead parametric studies without the need of any fitting/adjustment parameters.

Our parametric study shows that the maximum pull-in voltage drift is managed by the number of available traps inside the dielectrics; whereas the trapping kinetics can be monitored by more parameters such as the conduction current, the capture cross-section and the switch design. In conclusion, the best way to

reduce drastically the dielectric charging at long term requires the reduction of the available traps either by improving the dielectrics properties (difficult task due to PECVD process), or by reducing the dielectric volume. Consequently, CEA-LETI has chosen the second option and has developed a dielectric-less version of its electrostatic ohmic switch [2]. Our switch is still made of a nitride membrane with a central gold contact and pairs of electrodes on both sides but the insulated layer between the actuation electrodes has been removed mechanical blocks and have been implemented to avoid the direct contact between electrodes (see Fig.2). The first results are very promising because no significant pull in voltage drift has been observed after 500 hours of constant voltage stress.



Figure 1. Measured and simulated pull-in voltage drift for PECVD SiNx dielectric materials.



Figure 2. Dielectric-less version of the electrostatic ohmic switch.

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Annual Research Report 2011 Silicon Technologies & Components



3D Integration & Packaging

- Vias Technologies for Through Silicon Vertical Interconnections
- Advanced Material & Processes for Through Silicon Via Filling
- Reliability of Polymer Filling Integration for 3D-Via Last
- Performances of Wafer-Level UnderFill with 50µm Pitch Interconnections
- Reliability of 200°C Direct Bonding Copper Interconnects
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Vias Technologies for Through Silicon Vertical Interconnections

Research Topics : 3D Integration, TSV, Via-First, Via-Middle

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As miniaturization of the CMOS components are becoming more and more difficult and costly new fields for improving the ICs performances are actively developed. One of the most promising ways is certainly the 3D integration of stacked chips. Through Silicon Vias (TSV) is a key technology to go to 3D device stacking. Different integration schemes have been proposed, but no single solution has emerged as yet. The choice to make the TSVs before or during the devices fabrication (via-first or via-mid approaches) or after (via-last approach) will mainly depend on the constraints of the final product.

This work is primarily focused on the development of the different via-first and via-mid TSVs technologies. In the first case, thermal oxide and highly doped polysilicon are respectively used as the materials for isolation and metallization (Fig.1) since they are compatible with the subsequent fabrication of the transistors. Concerning the via-mid approach deposited conformal silicon oxide are likely to be used for isolation as well as tungsten (Fig.2) or copper (Fig.3) for the metallization. The main technical challenges rely on the etching and the filling with the isolation and metallization materials for structures having a very high aspect ratio (AR), typically width of 10 μ m for a depth of 100 μ m (AR10).

In each case, every process steps was optimized including the deep silicon etching, the filling of the structures with insulations and metals layers, the contacts on the front side as well on the thinned substrate backside. Complete integrations have been achieved using dedicated test vehicles and electrical outputs were successfully obtained with resistance values conform to expectations and high daisy chain yields.

TSV thermo-mechanical behaviors were also thoroughly investigated in each case using in line process monitoring like wafer curvature measurements as well as localized physical characterizations at the TSV scale like chemical defect decoration, Electron Back-Scattered Diffraction (EBSD), X-Ray diffraction (XRD) and μ Raman. These experimental findings were found to be in good agreement with finite element modeling and finally accredit the compatibility of the TSV features along with the transistors.



Figure 1. TSV via-first filled with doped polysilicon.







Figure 3. TSV via-mid filled with copper.

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Advanced Material & Processes for Through Silicon Via Filling

Research Topics : 3D Integration, TSV, Via Filling

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Partnership : STMicroelectronics, CPE LYON

Recently, 3D integration using Through Silicon Vias (TSVs) has attracted much interest for the next generation of microelectronics devices. The TSV architecture key challenge is the achievement of a metallization that properly fills TSVs with high aspect ratio (AR>5). In many applications, TSVs are filled with copper. This metallization proceeds through 3 main steps, (i) barrier layer (typically TaN) deposition, (ii) Cu seed layer deposition and (iii) Cu electroplating.

The latter step ensures void-free filling of the features thanks to specific additives that promote 'superconformal' or bottom-up deposition. However, this step relies on the quality of the underlying barrier and seed layers, which are currently deposited by Physical Vapour Deposition (PVD). In this technique, matter flux is highly directional, which causes very limited coverage of the vertical TSV sidewalls, eventually leading to discontinuous coatings. Therefore, processes based on chemical reactions conducted in liquid solutions can be used to get a more conformal film.

For Cu seed layer deposition, a Direct on Barrier (DoB) electroplating (ECD) process has been investigated as an alternative to PVD [1]. In this approach, Cu is electroplated directly on the diffusion barrier layer despite its high electrical resistance and superficial oxidation under air. This superficial oxide can be removed by electrochemical reduction conducted in a supporting electrolyte. This treatment limits oxygen content at the barrier/Cu interface and significantly improves Cu nucleation. As a result, highly conformal films could be obtained, which allowed reducing nominal thickness of the Cu seed layer from 1 µm to less than 150 nm while preserving sidewalls film continuity (Fig.1).



Figure 1. Cu seed layer formed by a DoB ECD process.

Metal barrier deposition onto an insulating material is even more challenging. To achieve this, a specific strategy was devised [2], which uses a surface preparation by hydroxylation of the SiO₂ surface, followed by a self-assembled monolayer (SAM) deposition using a silanization reaction. This organic layer promotes the chemical deposition of an extremely thin Pd activation layer, which catalyzes the electroless deposition of binary or ternary Co- or Nibased alloys. Pd activation and NiP electroless deposition was successfully conducted on top of this SAM leading to conformal, 100-150 nm thick sticking NiP layer (Fig.2).



Figure 2. NiP barrier layer in a 8:1 aspect-ratio TSV.

A more advanced strategy to address both barrier and seed layer deposition would be to (i) synthesize nanoparticles of the metals and (ii) deposit these nanoparticles onto the dielectric material to form the desired layers. Thus, we have recently reported a new and versatile synthesis of size-controlled bimetallic nanoparticles using Cu and Ru precursors in ionic liquids [3]. Smaller bimetallic nanoparticles (1.9 to 2.8 nm) are formed as compared to single metals (Cu: 5 nm; Ru: 4 nm) with enhanced size control in a large range of Cu molar fraction (Fig.3).



Figure 3. Size evolution of RuCu NPs with $\mbox{Cu:Ru}$ ratio in the solution.

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Reliability of Polymer Filling Integration for 3D-Via Last

Research Topics : 3D Integration, Assembly, Through Silicon Via, Reliability

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Partnership : STMicroelectronics, IM2NP, ShinEtsu

Through silicon via is one of the key technologies that enable 3D integration [1]. For packaging applications, preferred integration scheme remains via last approach, meaning building via after BEOL-CMOS, mainly for cost considerations and when direct access to CMOS design is not possible. This work focus on typical medium density TSVs (A.R.2, Ø60µm, 120µm deep) which are partially filled with thick copper liner deposited by ECD. These electrical paths dedicated to signal redistribution are insulated with liquid polymers deposited by spin on process, inducing air trapping inside the TSV. Thus, in this area, copper may be subject to oxidation. This behavior is amplified by membrane cracking on top of the TSV (Fig.1). Polymer filling of via is presented as a way to gain reliable and 3D-ready structures [2].



Figure 1. Cross-section and top view SEM pictures of TSVs with copper RDL and passivation layers.

Polymer filling can be achieved with normal spin on process of a liquid polymer, followed by a calibrated vacuum heating. Polymer viscosity decreases, allowing air removal inside the TSVs. Other method consists in vacuum lamination of a dry film resist, performing better uniformity and process control.



Figure 2. Cross-section of a polymer filled TSV and simulated radial stress profile at the TSV bottom.

CTE mismatch between the polymer and surrounding materials may produce high stress inside the TSV. Thus, 2D axis-symmetric model is developed (Fig.2) in order to calculate the thermo mechanical stress generated at room temperature. Result shows higher stress values at the TSV bottom edge, near BEOL structures, pointing out a risk of failure in this area. To confirm this result, reliability of the polymer filled TSV structure is thus investigated [3] through electrical tests coupled with harsh thermal cycling according to JEDEC standards. Temperature varies from -40° C to 150° C with a 10 min soak time. Then, a comparison is performed with spin on insulation.

Firstly, comb-serpentine structures included in the RDL shows no leakage current variation during cycles with a mean value of $95\pm5pA$ with both encapsulations. This result indicates no degradation of the dielectric properties of the polymers.

Kelvin test pattern allows TSV resistance monitoring at regular intervals. Spin on encapsulation demonstrates resistance degradation with cycles. A morphological analysis highlighted copper oxidation inside the TSV. No resistance variation is noted with polymer filled via (Fig.3), demonstrating better copper passivation behavior.



Figure 3. TSV resistance evolution (Kelvin pattern)-standard insulation (left) versus via filling (right).



Figure 4. 100 TSVs chains resistance evolution - standard insulation (left) vs. via filling (right).

Chains of 100 TSVs are also investigated (Fig.4) in order to check structure reliability. Polymer filled via demonstrated higher failure rate when compared to conventional encapsulation. Morphological post mortem analysis demonstrated copper cracking at via bottom, matching perfectly with previously simulated results. Two ways are proposed to overcome this issue: increase of copper thickness inside the TSVs to gain better rigidity and use of composite polymers filled with SiO2 or SiN nano particles.

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Performances of Wafer-Level UnderFill with 50µm Pitch Interconnections

Research Topics : 3D Integration

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Partnership : STMicroelectronics, Sumitomo Bakelite

Up to now, the conventional underfilling process has relied on the capillary flow of the underfill resin between top and bottom dies. However, the continuous interconnects dimension and gap reduction of 3D technologies will limit the use of Capillary Underfill (CUF) for future applications. Therefore, to overcome dimension problems and ensure process throughput, several pre-applied underfill materials have been developed. Among them, Wafer-Level UnderFill (WLUF) is one of the most promising techniques. Indeed, by acting at wafer scale, contrary to Non-Conductive Paste (NCP), its main advantage is the throughput increase as material deposition and flip-chip mounting can be achieved on two separate tools.

The target of the work achieved at LETI [1] is to demonstrate dry-film WLUF process and performances for fine micro-bumps interconnect (22µm high separated by 50µm) in a silicon to silicon flip-chip stacking. Furthermore, WLUF performances in thermal and humidity cycling have been compared with a standard CUF used in the industry, on the similar 50µm pitch structures (Table 1).

Tuble 1. Under mis properties.			
Item	CUF	WLUF	
CTE (α1)	38	40	
	ppm/°C	ppm/°C	
CTE (a2)	135	150	
	ppm/°C	ppm/°C	
Modulus	6 GPa	4 GPa	
(30°C)			
Тg	120 °C	120 °C	
Filler	50%	50%	
content	weight	weight	

Table 1. Underfills properties.

Test vehicles for electrical connections behavior study are performed with 1812 peripheral and 374 central interconnects. Top die micro-bumps consist in copper pillars with 25µm diameter, 50µm pitch, 10µm high Cu and a 12µm thick SnAgCu(SAC) solder cap. The corresponding bottom substrate presents 10µm high copper posts.

A total of 80 CUF dies and 28 WLUF dies have been assembled in collaboration with our partners, and we firstly achieved a cross-section of each die type to assess the good interconnection formation after flipchip (Fig.1).

After assessing the void free polymeric interface, the length of the fillet and the initial performances of the interconnections, all the dies have been exposed to JEDEC-MSL 4 preconditioning followed by temperature cycling (TCT) or moisture storage.



Figure 1. Cross-sectional photo after chip assembly: with CU F (left), with WLUF (right).

Electrical resistance of various interconnection daisy chains has been measured after increasing cycles number.

Resistance evolution during thermal cycling of the most critical 100 interconnections chain is shown in Fig.2. It can be seen that whatever WLUF or CUF average normalized resistance curves present similar and in-specifications values demonstrating WLUF performances in 50µm pitch stacks. A similar behavior has been observed on dies exposed to moisture storage up to 1000 hours.

Shear tests processed on dies after thermal and moisture tests have revealed that the shear force required to separate stacks glued by WLUF is higher than those requisited to separate CUF stacks. In addition, WLUF failure mode observed is top die breakage, whereas CUF failure mode is underfill delamination, demonstrating WLUF higher adhesion on silicon.



Figure 2. Normalized resistance deviation after TCT for a 100 copper pillars chain.

These innovative results tend to demonstrate that WLUF is pertinent as underfill for fine micro-bumps interconnect in a silicon to silicon flip-chip stacking and will be a relevant technology for the future integrations. Further tests are in progress to understand the impact of process parameters on WLUF performance.

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Reliability of 200°C Direct Bonding Copper Interconnects

Research Topics : 3D Integration, Direct Bonding, Reliability

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Partnership : Lyon University, ENISE

The three-dimensional integration appears as a good alternative solution to overcome the limitation of the component miniaturisation (Moore's law) and thus allow the devices performance to increase. To create 3D interconnects the metal direct bonding has the advantage to lead to an isolated vertical electrical contact with a high bonding strength. Results on direct copper bonding have already been published as a promising way to interconnect strata. Reliability of 200°C copper bonded daisy chains are tested [1]. The number of connections varies from hundred to around 30000 interconnections Fig.1 illustrates a 2mm² chip with an interconnection density as high as 1.5 10⁶ /cm².



Figure 1. FIB SEM observation of a daisy chain DC5.

Thermal cycling

200°C Daisy chains were subjected to a thousand thermal cycles from -65°C to +150°C. No degradation of resistance was recorded from all the different structures tested : from 1 to 30K connections, from 3 to 10 μ m width and for symmetrical or asymmetrical Daisy chains. The bonded interface is thus stable enough at 200°C to pass these tests see Fig.2.



Figure 2. Thermal cycling test (TCT). Cumulative resistance on Daisy chain DC3 subjected to 500 and 1000 thermal cycles.

<u>Stress induced voiding (SIV) test on 200°C post</u> <u>bonding annealed samples</u>

SIV test was carried out at a thermal stress of 175°C for 500h on various Daisy chains. Resistance measurements were done before and after storage, and represented on Fig.3. In this case, 99% of the tested dies had a positive shift resistance of less than

3%. Another important result to note is that even with long anneal no short circuit occurred. So copper diffusion, into the oxide, if any, do not degrade the structure even with a pitch as low as 7 μ m.



Figure 3. Cumulative probability of Daisy chain resistance before and after baking at 175°C for 500h.

Package level electromigration test

EM tests (Fig.4) were achieved on packaged Daisy chains, whose that have been subjected to a 200°C post bonding anneal. Each device underwent two temperatures (325 and 350°C) and two current stress conditions (3 and 3.5 MA/cm²). The time to failure (TTF) is obtained for a 10% resistance variation. Only one degradation phenomenon was observed and was linked to a lack of adhesion of copper seed layer on TiN and not to the bonding interface.



Figure 4. EM tests on Daisy chain for two temperatures and two current densities.

Through these reliability studies, direct copper bonding appears as a promising solution for metallic interconnection used on various applications as 3D integration, MEMS sealing or power devices.

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Chip-to-Wafer Direct Bonding for High Density 3D Integration

Research Topics : 3D Integration, Direct Bonding, Chip to Wafer

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Sponsorship : MINALOGIC-PROCEED

Partnership : SET, STMicroelectronics, Air Liquide Electronic Systems, CNRS-CEMES

3D integration has originated from the need for an economically viable scheme to achieve innovative multifunction systems through the assembly of heterogeneous existing sub-parts. Chip-to-Wafer (CtW) technologies are a promising solution for high density 3D integration application to overcome the limitation of Wafer-to-Wafer assembly in terms of stacking yield, alignment accuracy and reproducibility along the wafers.

Direct bonding has emerged as a powerful technique in the field of substrate engineering. In particular, direct Cu bonding was developed at Leti to enable the assembly of Cu/SiO₂ damascene-patterned surfaces. Direct bonding is especially attractive as it is performed at room temperature, low pressure and it avoids pre- or post-bonding underfill even for a high interconnection density.

For the first time, we have demonstrated CtW assembly based on direct bonding (Fig.1) for Cu/SiO_2 damascene-patterned surfaces. This work was performed in the frame of the FUI- and FEDER-funded "PROCEED" Minalogic project.



Figure 1. Chip-to-wafer assembly by direct bonding.

This achievement required the completion of four distinct tasks: (*i*) the development of dedicated pickand-place equipment, (*ii*) the understanding of the bonding mechanisms, (*iii*) the elaboration of a suitable surface preparation sequence and (*iv*) the assessment of electrical continuity between wafer and die.

SET developed a pick-and-place equipment that allows sub-1µm alignment. Thanks to special design, particulate contamination is controlled to a level that is compatible with direct bonding.

The bonding sequence consists in two steps. During the first step, the pick-and-place tool accurately positions the die on its corresponding wafer hosting site. At that point, the die situation is secured by the direct bonding of SiO_2 surfaces that occurs at room temperature. After complete die populating of the wafer, the second bonding step takes place during an atmospheric collective thermal treatment that promotes linking of Cu surfaces. In the course of that step, Cu grain boundaries change through the creation of diffusion cones at the bonding interface (Fig.2), to the benefit of adhesion and of electrical continuity.



Figure 2. TEM imaging showing structural evolution of the Cu bond upon annealing.

Surface preparation towards die-to-wafer direct bonding includes the elaboration of mirror-polished properly terminated surfaces and the dicing process sequence. These technology developments are guided by the specific requirements on one side of collective die handling up to the pick-and-place operation, and on another side of the surface preparation for direct patterned metallic/oxide bonding.

Finally, electrical continuity measurements show that Cu interconnects fabricated through CtW direct bonding have a tightly distributed resistivity (Fig.3). Moreover, this value is identical to the value without bonding

These results pave the way towards high-density 3D integration.



Figure 3. Electrical characterization of contact chains formed by die-to-wafer \mbox{Cu}/\mbox{SiO}_2 direct bonding.

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3D SIP based on TSV and Micro-Insert Interconnections for Smart Card Applications

Research Topics : 3D Integration, Wafer Level Packaging, Interconnections

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Sponsorship : SCS-SMARTSTACK

Partnership : STMicroelectronics, ENSM.SE, Fogale, EPTS, Gemalto

The 3D packaging has to satisfy high interconnection density, high data throughput with good signal integrity, and reliability which lead to combine disparate technologies such as thinning, Through Silicon Vias (TSV) and dies interconnection. All these developments were studied in a project called SmartStack which goal was to address 3D technologies for smartcard application.

A via last approach was chosen to be compatible with die integration coming from various foundries. As a consequence, the TSV process was performed on the wafer backside after thinning.

The interconnection between each die was based on chip on wafer bonding and micro-inserts technology (Fig.1). Small spikes of Ni are formed at the interconnection point between the two circuits. The approach allows a very narrow connection (less than 10 μ m interface) and do not require any underfill.



Figure 1. Schematic view of interconnection using micro-inserts.

A test vehicle which allows characterizing the required technologies has been designed and manufactured. It consists of two dies (top and bottom die) including TSV and pads redistribution on both sides (Fig.2). These dies are stacked on silicon interconnection network which allows extracting electrical signal on the PCB through wire bonding. The electrical continuity through the stacking was tested from the silicon substrate thanks to daisy chain.



Figure 2. Schematic view of the test vehicle.

To explore the limit of the "via last" technology, the test vehicle was designed with different geometries including tapered via (Fig.3). Both side of wafer contain metal structures which constitute a contact daisy-chain testable at the wafer level from backside.



Figure 3. Test vehicle layout.

Scanning Electron Microscopy (SEM) cross-sections of TSV were performed and have demonstrated a good continuous coverage of SiON layer and Cu layer on sidewall and via bottom. More than 97% of die have presented an electrical continuity through daisy-chain for TSV of 50 microns in diameter (Fig.4).



Figure 4. SEM view of TSV cross section.

Thanks to our partners dedicated metrologies were introduced to study the stress and morphology.

Stacking was performed in two steps. All dies were attached with the flip-chip tool and then collectively bonded using a EVG 520IS Thermo-compression. Microinsert between dies was demonstrated to be efficient as electrical link and in compacting the clearance between two subsequent dies (Fig.5).



Figure 5. 200mm test vehicle wafer with 223 dies stacked.

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Multi-Layers Non Evaporable Getters Thin Films for MEMS Wafer Level Packaging

Research Topics : MEMS Packaging, Atmosphere Control, Getter

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It is now well established that thin film Non-Evaporable Getters (NEG) are necessary to ensure atmosphere control in a MEMS cavity. It is also well known that the getter effect is in relationship with the microstructure of the film and is enhanced when structure is columnar with small grain size. NEG play a main part which consists in absorbing gases released during first the packaging process, and second all along the component life-time. According to the Wafer level Packaging (WLP) process, either by wafer to wafer bonding or by thin film encapsulation, the thin film getter is exposed to different gases that could be detrimental for its sorbing capacity. Leti is working on both technologies and has developed a wide range of thin film getters [1], considering their activation temperature and chemical compatibility with The getter properties are packaging processes. partially controlled with a metallic sub-layer and the relevant question is to evaluate its impact on the microstructure of the getter layer.

Basic researches [2,3] undergone to better understand this multi-layers NEG behavior has been focused on microstructure observation by Transmission Electron Microscopy (TEM).

Fig.1 illustrates the modification of the titanium getter layer by a platinum sub-layer. In both cases a columnar structure with a strong Ti (0002) texture is observed for the first part of the layers. Grain enlargement is clearly put forward for the remaining upper part of the getter. However, the top grains for the Pt\Ti stack are V-shaped with larger grain size than for the Si\Ti stack, and their crystallographic orientation is different from the textured part layer. Moreover, for this Pt\Ti deposit, inter and intragranular cavities are observed. Fig.2 corresponds to the previous deposits after an activation cycle under nitrogen at 450°C. In both cases, microstructure is mainly modified compared to as-deposited getters. For the Pt\Ti deposit, the Ti layer is strongly (0002) textured (Fig.2 bottom) and vertical dislocations lines are observed while grain size are about twice the grain size of the Ti layer on silicon (Fig.2 top).

For the latter dislocations lines are also observed but the (0002) texture is not so marked.



Figure 1. TEM dark field image of Si\Ti (top) and Pt\Ti (bottom) stacks as deposited.



Figure 2. TEM dark field image of Si\Ti (top) and Pt\Ti (bottom) stacks after exposure to nitrogen at 450° C.

According to these results, dislocations lines might be a contributor to the getter effect. Further observations need to be performed to better assess this assumption.

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Physical & Chemical Characterization

- Quantitative Depth Profiling of Ultrathin High-k Stacks with Full Spectrum Time of Flight-Secondary Ion Mass Spectrometry
- Kelvin Force Microscopy Characterization of Charge Trap Layers for Non-Volatile Memory Applications
- The Auger Nanoprobe for Surface Chemical Characterization at the Nanometer Scale
- Advanced Backside Sample Preparation for Multi-Technique Surface Analysis
- Strain Mapping with nm-Resolution by Dark-Field Electron Holography
- Field Mapping in an Electron Microscope for SOI Device Technology with 1 nm Spatial Resolution
- CMP Metrology for Advanced FEOL Processes
- FOUP to Wafers Molecular Cross-Contamination
- Use of TXRF to Monitor Ultra-Thin Lanthanum Oxide Layers in Complex High-k Metal Gate Stacks

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Annual Research Report 2011 Silicon Technologies & Components

Quantitative Depth Profiling of Ultrathin High-k Stacks with Full Spectrum Time of Flight-Secondary Ion Mass Spectrometry

Research Topics : Surface Characterization

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Sponsorship : Uttermost, RTB, Kyoto-Advanced Nanotechnology Network

Partnership : STMicroelectronics, LTM-CNRS, INPG, Kyoto University

A new analysis protocol, called the Full Spectrum protocol, has been developed for the Time of Flight-Secondary Ion Mass Spectrometry (ToF-SIMS) analysis of gate stacks and SiGe layers. Compared to standard ToF-SIMS protocols, the full spectrum protocol allows simultaneous quantification of all major elements present in the sample with reduced matrix effects. Fig.1 shows the effect of using the Full Spectrum protocol on a thin SiON layer. Instead of measuring just the Si- ion, all silicon containing ions are measured and summed to give a total silicon signal Q_{Si} that is more representative of the actual silicon distribution. When several elements are present the same procedure is repeated for each element, and sensitivity factors are calculated using known reference samples.



Figure 1. ToF-SIMS Profile of a 1.9 nm thick SiON layer on a Si substrate, in which the intensity of several Si containing ions are plotted as a function of depth. The signal Q_{Si} is the sum of all silicon containing signals.

Here we shall concentrate on the application of the full spectrum protocol to high-k gate stacks, for which SIMS or ToF-SIMS characterization is still hampered by various matrix effects and the comparison with other well established methods to confirm the accuracy of the Full spectrum method such as High resolution Backscattering Spectrometry (HRBS) and parallel Angle Resolved-X-ray Photoelectron Spectroscopy (pAR-XPS) which have already proven their ability in this domain. Elemental concentration depth profiles of high-k material stacks for 32 nm nodes devices and below were acquired by HRBS, pAR-XPS and ToF-SIMS. Three different samples were studied in this work, one ultra-thin Insulating Layer (IL) alone, and two nitridized high-k/IL samples with different nitridation conditions for the IL. Comparison of the elemental profiles obtained by all three techniques allows the accuracy of the Full Spectrum ToF-SIMS protocol to be assessed, both in terms of chemical composition quantification and depth resolution as is shown in Fig.2.



Figure 2. Overlaid full-spectrum ToF-SIMS, HRBS, and pARXPS profiles of the HfSiON/SiON/Si sample.

The results from ToF-SIMS, HRBS and pAR-XPS the three techniques are in good agreement. However, some slight differences are observed, especially in the nitrogen level in the hafnium silicate layers, which requires further investigation. This study reveals the feasibility of quantitative and depth resolved ToF-SIMS profiling of ultra-thin high-k material stacks [1] The full spectrum method has also proved valuable for simultaneous matrix and dopant quantification in SiGe layers [2-4] For example the accurate quantification provided by the Full Spectrum ToF-SIMS protocol has been useful in characterising the test samples used in the development or the Dark-field holography strain mapping technique.

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Kelvin Force Microscopy Characterization of Charge Trap Layers for Non Volatile Memory Applications

Research Topics : Surface Characterization

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Partnership : UTTM

Silicon nitride (Si_3N_4) and silicon nanocrystals are actively being researched for near-future replacement of the continuous polysilicon floating gate in NAND flash memory. Their main advantage over a continuous polysilicon floating gate is discrete charge trapping that allows the reduction of the memory cell dimension. Indeed discrete charge trapping layers exhibit a very good robustness against SILC effect (Stress Induced Leakage Current) and therefore allow a thinner tunnel oxide.

For this purpose, we have analysed various samples: SiO_2 (as reference sample), Si_3N_4 (6 nm thick) film deposited on SiO_2 , silicon nanocrystals with and without silicon nitride cap [1].



Figure 1. Cross-section profiles of 6-nm Si₃N₄ surface potential taken immediately after charging (here, we show measurement for a positively charged tip). Charging of the sample was made after baking under nitrogen to 120 °C and cooled down within half (thick line), one (thin line), and four (dotted line) hours under nitrogen flux. Inset is showing the topography of Si₃N₄ surface (circle is showing charged area) and equivalent KFM surface potential measurement (line is indication of the data used as cross-section z-scale of the topography image).

Here, we present a study of the dynamics of charge injection in SiN based test structures using Kelvin Force Microscopy (KFM). KFM is one of the techniques used to detect the surface potential (V_s). In KFM, an electrostatic excitation (DC+AC voltage) is applied to the tip at the cantilever resonance frequency. The electrostatic excitation generates a cantilever oscillation (or resonance frequency shift) if the cantilever DC bias does not match the sample surface potential V_s. To measure V_s, a feedback is introduced so as to nullify the cantilever oscillation frequency (or frequency shift) at the electrostatic excitation angular

frequency. This generates a map of the surface potential V_s (see Fig.1).

We made a set of measurements done by KFM under flowing gaseous nitrogen and we compare these results with KFM performed in Ultra High Vacuum (UHV). Under UHV we observe the "genuine" behaviour of the material, as there is complete absence of moisture or any adsorbed contaminants. We experimentally prove that all samples charged under UHV conditions show much better retention than in ambience. Such measurements demonstrate that surface contamination and moisture dominate during discharging process and adversely affects the storage capacity [2].

Moreover, by using an analytical formula [3] we achieved numerical simulations to calculate amount of total injected charge (see Fig.2).



Figure 2. Charge density calculated from KFM potential images using Poisson solver (see inset). Measurement was done for various time of charging and Si_3N_4 (6 nm) sample surface. Logarithmic fit was used to indicate charge saturation.

Summarizing, we compare charging experiments made under different conditions (nitrogen, UHV) and with different experimental KFM setups (amplitude and frequency modulation KFM). Finally, from our surface potential measurements we extract amount of injected charge.

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The Auger Nanoprobe for Surface Chemical Characterization at the Nanometer Scale

Research Topics : Surface Characterization

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Sponsorship : ANR-RTB

Partnership : CEA-LITEN, Institut Lavoisier (CNRS)

Complex architectures of functional materials based on nano-structures or thin multilayers stacks are currently developed for nanotechnologies. Advanced characterization techniques are needed at the nanometer scale. Auger spectroscopy and microscopy have gained interest for the analysis of surface elemental and chemical composition, thanks to recent improvements in lateral and energy resolutions. Indeed, state-of-the-art Auger nano-probes combine small probe sizes (<10 nm) with high energy resolution (0.1 %). Surface sensitivity makes it complementary to electron microscopy techniques (EDX and EELS) and higher spatial resolution offers an alternative to photoelectron spectromicroscopy (XPEEM).

In June 2010, a state-of-the-art PHI 700Xi Auger nanoprobe (Physical Electronics) was delivered at the Minatec Nanocaracterization Centre (NCC). Spatial resolutions for Secondary Electron Microscopy (SEM) and Auger Scanning Microscopy (SAM) were shown to be as low as 6 and 8 nm, respectively. The instrument design (co-axial geometry), as well as recent improvements (isolation enclosure), offer high and uniform sensitivity (0.1 at. %), high spatial resolution and long term stability. Depth resolution (<2 nm) is also improved by a new floating ion gun allowing low energy sputtering.

The performances of this nanoprobe in terms of spatial sensitivity are illustrated via the analysis of semiconducting $AI_{0.7}Ga_{0.3}As/GaAs$ multilayers with certified patterns at the deca-nanometric scale and chemically sharp interfaces (see Fig.1). High spatial sensitivity is achieved at 25 kV/1nA with clear identification of $AI_{0.7}Ga_{0.3}As$ layers as thin as 4 nm.



Figure 1. Auger line scans of AI (KLL) and Ga (LMM) peaks intensity along the $AI_{0.7}Ga_{0.3}As/GaAs$ structures measured at 25kV/1nA; inset: SEM image.

ZnO nanowires are promising structures for optoelectronic devices such as light emission sources (LEDs). They are extensively characterized by electron microscopy techniques. However, EELS and EDX can only provide the bulk elemental composition. Highresolution Auger microscopy helps to analyse the surface chemical composition, in terms of spatial distribution (see Fig.2).



Figure 2. Auger mapping of a ZnO nanowire on Si, with the corresponding SEM image and Zn profile.

A cluster system for surface imaging was also made possible with an independent reactivity chamber enabling UHV transfers to high resolution XPS, XPEEM and AFM instruments. Combined surface analyses are therefore possible from the micro to the nanometer scale (see Fig.3) with meaningful complementary information.



Figure 3. The Auger nanoprobe as part of the cluster system for surface imaging at Minatec NCC.

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Advanced Backside Sample Preparation for Multi-Technique Surface Analysis

Research Topics : Surface Characterization

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Partnership : STMicroelectronics, CNRS-LTM, INAC

In microelectronics the combination of dimensional scaling and the integration of new materials in the standard gate stack for the 32 nm nodes and below, make it increasingly difficult to draw accurate conclusions from conventional front-side surface analysis. Backside preparation is one of the solutions which can help solve this problem. However in the case of such thin layers, the sample preparation remains challenging since, starting from the whole sample on thick substrate, only a few tenths of nanometers corresponding to the layers of interest must remain while maintaining a smooth and flat surface suitable for analysis. A simple method for backside sample preparation adapted to samples grown on Si substrates and containing sub-nanometer ultrathin pedestal oxides has been developed. It consists in a mechanical polishing down to a few remaining microns, followed by a dedicated TetraMethylAmmonium Hydroxide etch. The preparation process is described in Fig.1.



Figure 1. Schematic representation of the different steps in the backside preparation process. [1].

We used it to prepare samples consisting of highk/metal gate stacks for 32 nm node Complementary Metal Oxide Semiconductor devices. The samples are composed of the following layer stack, starting from the Si substrate, (i) a thin SiON (1.5 nm) layer (etch stop layer), (ii) an HfSiON (1.7 nm) layer, (iii) a 0.4 nm lanthanum oxide layer, (iv) a 6.5 nm thick TiN gate and (v) a 60 nm thick Poly Si capping. Physical characterization of both unprepared and backside prepared samples was performed using several techniques to investigate the results yielded by the preparation. Time of Flight SIMS (ToF-SIMS) depth profiling was performed with a TOF SIMS V tool from ION-TOF GmbH. Medium Energy Ion Scattering experiments were carried out on a 400kV accelerator from HVEE coupled to an ultrahigh vacuum analysis chamber. Samples were also analyzed with a customized Theta 300 X-ray photoelectron spectrometer from Thermo Fisher Scientific with parallel angle resolved capability. Fig.2 shows the profiles obtained by ToF-SIMS on the same highk/metal gate sample, using frontside and backside analysis.



Figure 2. ToF-SIMS profiles of the same high-k/metal gate sample, with both frontside and backside approaches.

Both approaches yield similar profiles in the TiN region at least in terms of sputter rate, given the good alignment of the profiles in this region. However there is huge horizontal scale distortion in the right region of the image, corresponding to the HfSiON and beneath layers. This is a direct effect of the Hf segregation during analysis, known analytical artefact for this kind of samples. The same effect is not observed on the backside profile. The accuracy of ToF-SIMS analysis on this kind of sample is thus greatly enhanced by using the backside preparation approach proposed in this work, yielding more realist elemental distributions in the stack and allowing quantitative studies to be done [2].

Similar improvements were obtained for the other characterization techniques, or in some cases backside analysis is the only way to achieve meaningful results on the high-k layer. The combination of techniques enabled the La distribution, an important parameter in determining the performance of such stack to be finely characterised.

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Strain Mapping with nm-Resolution by Dark-Field Electron Holography

Research Topics : Electron Microscopy, Strain Engineering

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Sponsorship : ANR-RTB

Partnership : STMicroelectronics, IBM Fishkill

As strain is now used routinely in transistor devices to increase the mobility of the charge carriers, the microelectronics industry needs techniques that can map the strain with nanometer resolution. Dark-field electron holography (DFEH) is one of the most promising techniques for measuring strain in semiconductor devices with high resolution and sensitivity. DFEH is set up in a transmission electron microscope. The principle is to interfere electron beams that have been diffracted by both the strained region of interest and the substrate using an electron biprism.

In order to assess the performances of DFEH for quantitative strain measurement, calibration samples of SiGe layers were first examined (Fig.1). When grown on Si by epitaxy, thin SiGe layers are tensily strained in the growth direction due to the lattice mismatch between Si and Ge. Several measurements were performed on samples of different Ge content (a,b). The Ge concentration was determined using ToF-SIMS and the strain in the layers was then simulated using finite element modelling (c). A good agreement was found between experiment and simulation in a range of $\pm 0.1\%$ for [Ge]<25% and $\pm 0.2\%$ for [Ge]>25%. More examples of strain measurements in SiGe(C) thin layers can be found in [1].



Figure 1. Strain measurement in SiGe layers grown on Si substrate. (a) Strain maps. (b) Strain profiles extracted from the maps in the growth direction. (c) Simulated strain profiles.

DFEH was then applied to the characterization of strained devices (Fig.2). SiN contact etch stop layers (CESL) and SiGe source/drain (SD) are two processes that are used to introduce uniaxial strain. Here we have investigated the addititvity of these two processes. Three different situations were considered (a). First, dummy gates of 90 nm length were covered using a compressive CESL. Second, 50 nm deep recessed $Si_{0.65}Ge_{0.35}$ SD were grown by RP-CVD. Third, the two previous processes were combined (SiN & SiGe SD). Average strain profiles extracted from the channel as a function of depth are reported in (b). It was found that close to the gate, the sum of the strain of the two first cases (shown as dashed line) is close to the third case, confirming the additivity of the processes.



Figure 2. (a) Images and strain maps of uniaxially strained devices using compressive SiN CESL, $Si_{0.65}Ge_{0.35}$ source/drain, and both of them. (b) Average strain profiles extracted from the channel as a function of depth for the three different cases. The sum of the two first cases is reported as a dashed line.

In summary, DFEH can be used to map the strain at the nm-scale in thin layers or devices. As perspectives, correlations can be made with electrical measurements to understand the gain in charge carriers mobility. It can also help to improve the mechanical simulations of fully processed devices..

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Field Mapping in an Electron Microscope for SOI Technology with 1 nm Spatial Resolution

Research Topics : Electron Microscopy, Dopant Profiling, Strain Mapping

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Sponsorship : ANR-RTB, FEI Common Lab

Partnership : ST Microelectronics, IBM Fishkill

In order to develop the latest generations of semiconductor devices, it is essential to be able to obtain quantitative information about the structure, composition, dopant and strain fields. Indeed as the dimensions of these devices are reduced in size, it becomes increasingly important to have knowledge of all of these properties from the same samples as they interact with each other. However, although it is now straightforward to measure many of these properties in bulk devices; for devices that are grown using SOI technology we now need to develop new ways of characterisation. performing For example the rotational mismatch between the SOI film and the substrate makes strain mapping techniques such as dark field electron holography difficult to perform. Modern transmission electron microscopes are extremely stable and versatile which allows us to perform many different techniques during the same session. Here at LETI we use a first generation aberration corrected FEI Titan and the recently installed FEI Ultimate TEM which comprises two aberration correctors to give a spatial resolution of 50 pm. A monochromator and high speed electron energy loss (EELS) filter for compositional information about the specimens and an electron biprism to be able to measure the fields inside the devices [1]. The key to these experiments is the ability to provide high quality TEM specimens containing a single device that are prepared using back-side milling performed at a low operating energy in the focused ion beam.



Figure 1. (a) and (b) STEM images of a SiGe SOI pMOS device. (c) A strain map for the (001) growth direction.

Fig.1a shows a high-angle annular dark field (HAADF) scanning transmission electron microscopy (STEM) image of a sSOI/SiGe/Si pMOS device that is currently being developed. The SiGe/Si film is only 8 nm thick which makes characterisation challenging. Fig.1b shows a higher resolution image of the device, the SiGe films in the channel are brighter than the Si regions. Due to the stability of the TEM we are now able to measure the strain in the device directly from the STEM image using a technique known as geometrical

phase analysis [2]. A strain map for the (001) growth direction for the sSOI/SiGe/Si layers in the device is shown in Fig.1c. Here the spatial resolution is 1 nm and we can see that the lattice parameter is 0.7 % larger for the SiGe layers than for the Si regions in the specimen which is consistent with simulations. The strain map for the (110) growth direction (not shown here) indicates that there is no deformation, therefore the layers are all grown in perfect epitaxy with the sSOI layer.

To be able to obtain information about the electrostatic fields inside the specimen a technique called off-axis electron holography can be used. Until recently, the technique had a spatial resolution of around 6 nm for dopant profiling which made it unsuitable for the examination of modern device specimens. Now at LETI we have developed a method of performing electron holography to give maps of the electrostatic potential with a spatial resolution of 1 nm. Fig.2a shows a potential map in the device showing the location of the active dopants in the Source and Drain regions in the device. Fig.2b shows an EELS map giving the composition of the device. It can be seen that the channel comprises of only SiGe and Si and therefore any changes in potential in this region are due to the presence of active dopants. In SOI devices that contain many different materials in a region that is only a few tens of nanometres, information about the composition is vital if the electron holography results are to be correctly interpreted.



Figure 2. (a) A map of the electrostatic potential in the SiGe pMOS device. (b) EELS maps showing the composition of the device.

In summary, by taking advantage of the versatility of a state-of-the-art electron microscope we are able to recover structural, compositional and electrical information from the same specimen at the same time. The integration of many different techniques on the same TEM is powerful tool that can be used to understand and improve the performance of the future generations of microelectric devices.

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CMP Metrology for Advanced FEOL Process

Research Topics : Metrology, Haze Characterization

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Partnership : STMicroelectronics

In order to develop the latest generations of extended CMOS technology different approaches have been taken in the last years: Stress engineering, High K Metal Gates materials or lately Ultra-Thin body SOI and Fin FET structures. It is clear controlling the surface of such devices will be of paramount importance, aspects like roughness, surface quality, planarity in die and over the wafer will become more and more critical [1]. Very few techniques have the versatility to be nondestructive, fast, sensitivity enough and at the same time allow capturing die and wafer level information.

This work reports the first study of the diffuse background noise, or haze, as a fast indirect characterization technique on Chemical Mechanical Polishing (CMP) patterned wafers for advanced FEP process [2]. This technique, based on the diffusion and the diffraction of the light over the surface involves numerous contributions (e.g. roughness, refractive index, structure or even residues [3]) that lead to a very complex haze signal difficult to analyse. Nevertheless this choice is made because of the uncontested rapidity and sensitivity of the technique and the fact that a single process control step is sufficient.

CMP will become a critical process in gate last architecture integration. Indeed Replacement Metal Gate (RMG) process introduces two new CMP that will directly impact the critical gate height (-50 nm). The first expose the sacrificial poly-Si gate and call Poly Open (POC). The second polishing is a metal damascene CMP. Furthermore the specificities of the CMP process, variation in topography due to different densities and lines width, require measurements at die level but also quantification of the With In Die Non Uniformity (WIDNU) over the wafer.

Firstly, appropriate recipe has been developed in an KLA-Tencor SP1 tool (to start only one collection channel (wide) and one direction of light illumination (oblique) are used) to establish that haze has enough spatial resolution and sensitivity for CMP die-level characterization (Fig.1). Metallic covered wafers without polishing are then used in order to avoid in the haze signal the contributions due to the different materials. Fig.1 shows a good correlation between haze level and pattern density sample. Also nonuniformity of the CMP process on non-metallic covered wafers has been measured with haze and also characterized by thickness measurements on a Test Box Fig.2. From haze, map extraction of the haze's profile has been performed. Fig.3 shows a good correlation between haze and thickness measurements. Hence it has been demonstrated that spite of the fact

of pattern and their consequent complexity on the haze signal, it still a mean of monitoring under certain conditions specific process step. The former has the unique advantage to gather information at the wafer level but also at the die level in a fast measurement. Currently we are working in setting up statistical analysis over a large set of different use cases and implemented protocol analysis in order to avoid artefact and to have the more relevant data to implement a robust process control.



Figure 1. Haze level depending on density and position on wafer.



Figure 2. Haze map on pattern wafer and the associated thickness profile.



Figure 3. Profile of the haze level over a patterned wafer after stop on nitride POC CMP step process and thickness profile of SiO2 + SiN stack measured on thickness Test Box over the same wafer.

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FOUP to Wafers Molecular Cross-Contamination

Research Topics : Contaminants Behavior, Characterization

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Partnership : STMicroelectronics

Since FOUPs (Front Opening Universal Pod) constitute an enclosed environment made with porous plastics (mainly PC, PEEK, COP and PEI), they present specific molecular contamination issues for stored wafers. Indeed, such polymers are able to absorb volatile compounds coming from the connection to equipments or from the release from fresh processed wafers. The reversible outgassing of species previously trapped is also possible leading then to potential contamination of sensitive wafers and subsequent detrimental impacts.

This cross-contamination scheme, from air to FOUP and from FOUP to wafers, was clearly evidenced both for organics and volatile acids from lab studies [1,2] showing that the accumulation as the reversible outgassing are long-term phenomena (several days) governed by adsorption, solubility and diffusion laws. Moreover, corrosion or crystal growth issues on metallic layers due to molecular contaminants outgassed by FOUPs were largely reported. However, no study has characterized the exact nature and levels of the contaminants leading to such defects, and determined their sources along process flows.

In this goal, airborne molecular contaminants were characterized inside FOUPs between each process step along process sequences in real manufacturing conditions [3]. Two process flows were investigated, the Cu interconnect patterning (Fig.1a) and the lonic implantation of N-type or P-type dopants (Fig.1b) related to TiFx crystal growth on the TiN hard-mask and Poly-Si corrosion, respectively. Sensitive methods were used such as IMS, bubbling-IC, bubbling-ICPMS and TD-GCMS to measure respectively total acids, specific acids, volatile Si-species and organics.



Figure 1. Technical steps and defects studied a) Cu interconnects (after Line Etching) and b) N- or P-type dopants implantation (after Spacer Etching).

These molecular contaminants measurements clearly confirmed a correlation between acids detection in FOUP air and defects occurrence due to a FOUP to wafers cross-contamination mechanism (Tab.I). Moreover, for the first time to our knowledge, contaminants were clearly identified as HF, formic and acetic acids and quantified at levels of several tens of ppbv (Fig.2). Some process steps were also determined as contaminants sources. Thereby, dry etch and strip steps using F-gas are HF sources whereas acetic and formic acids are resists by-products obtained during implant, dry etch and strip steps. These original results allowed the targeted implementation of preventive (HF monitoring in FOUP, time constraints between process and curative (process FOUP steps) change, decontamination...) solutions along process flows.

Complementary works are currently pursued at the FOUP scale in order to evaluate and compare different FOUP materials in terms of contamination performances, decontamination ability... On the other hand, the contamination mechanisms of the FOUP's polymers by acids are characterized through the determination of the solubility and diffusion coefficients. This basic knowledge will allows a better understanding and quantitative assessment of these cross-contamination issues.

	With processed wafers	Wafers removed	
		t=0	1h after
FOUP A	45.2	≤ 0.2	22.6
FOUP B	34.5	≤ 0.2	13.7
FOUP C	100	≤ 0.2	45.0



Figure 2. Acids outgassed in an empty FOUP after different storage time (t_1) of processed wafers after the Cu line etch step (by bubbling-IC).

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Table I. Total acids in FOUPs after a dry etch step.

Use of TXRF to Monitor Ultra-thin Lanthanum Oxide Layers in Complex High-k Metal Gate Stacks

Research Topics : X-Ray Characterization

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Partnership : STMicroelectronics

Advanced nMOS gate stacks generally include a subnanometer lanthanum oxide cap layer between the dielectric and the metal layers so as to achieve the desired threshold voltage. The in-line metrology of the ultra-thin buried lanthanum oxide layer in complex high-k metal gate stacks grown on 300mm silicon wafers puts tight requirements on metrology tools and protocols. We have evaluated the capacity of Total X-Ray Fluorescence (TXRF) fab tools to monitor these complex stacks in a cleanroom environment.

The sample set included TiN/La2O3 systems grown by physical vapor deposition on HfSiON/SiON/Si stacks. The thickness of the lanthanum oxide layer was varied in the 0.4 to 1.2nm range while the thickness of the top TiN layer was set either to 1.0 or 6.5nm. The TXRF characterization was performed on Rigaku Fab300 tool operating with a tungsten rotating anode. At fixed incident energy (W-L, 9.67keV), the measurement conditions (glancing angle, measurement time) were tuned in order to improve the detection of the X-ray fluorescence of titanium and lanthanum elements. TXRF measurements demonstrated good sensitivity to lanthanum thickness variations along with limited dispersion deduced from reproducibility tests once the glancing angle exceeded the critical angle for total external reflection (Fig.1).



Figure 1. Intensity of La(Lb2) fluorescence line as a function of glancing angle.

As every indirect method, TXRF requires additional calibration process in order to convert the measured fluorescence intensity into thickness or dose information. We went through two possible calibration processes based on two reference techniques: the first one was based on the use of high-dynamic X-ray reflectometry (XRR) to get a reference value of the thickness of the lanthanum layer. Whereas the XRR spectra are significantly affected by the thickness variations of the lanthanum layer, XRR-deduced

thickness is highly unreliable (Fig.2) due to unexpectedly high correlation effects.



Figure 2. Discrepancy of XRR-deduced lanthanum thickness due to correlation effects.

The second calibration process was based on liquid phase decomposition of the stack using a specific acidic solution, followed by inductively-coupled plasma mass spectrometry (ICP-MS) analysis.

The promising results (Fig.3) and the clear tracks to decrease related uncertainty allow for considering the combination of TXRF and LPD-ICPMS to be a very effective solution to monitor sub-nanometer lanthanum-based layers in complex metal-gate stacks.





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